Solar-B **EIS** * EUV Imaging Spectrometer	Specification for the Solar-B EIS Read Out Electronics

Title	Specification for the Solar-B EIS Read Out Electronics
Doc ID	MSSL/SLB-EIS/SP05
ver	1.0
Author	Chris McFee
Date	3 April 2000

Contents

Change Record

Date	Issue	Section	Description of change

1 Introduction

1.1 Purpose

The purpose of this document is to establish the high level design for the Solar-B EIS Read Out Electronics (ROE). The system level requirements for the CCD camera (consisting of the Focal Plane Array (FPA) and the ROE is established in *MSSL/SLE-EIS/SP01* (reference [1]).

The FPA itself will consist of the CCD chip, and minimal electronics required to drive the CCD (level shifters) and pre-amplifiers to enable the small CCD signal to be processed at the ROE. The actual control of the CCD itself, such as generation of the appropriate clocking signal, and the measurement and digitisation of the CCD analogue output will be the responsibility of the ROE. The top-level design requirements for CCD control and measurement through the ROE are specified in this document.

1.2 Abbreviations

CCD Charge Coupled Device

CTE Charge Transfer Efficiency

EIS Extreme Ultraviolet Imaging Spectrometer

FPA Focal Plane Assembly

ICU Instrument Control Unit

ROE Read Out Electronics

1.3 Referenced Documents

1 EIS CCD camera - Systems Requirement Document - MSSL/SLB-EIS/SP01

2 Possible charge injection method. P. Pool, Marconi. Personal communication. December 1999.

2 Definitions

Frame - one CCD image, i.e, all the charge collected from the start of the integration period, to the end of this period.

3 ROE design requirements

3.1 Important CCD features

- The Marconi 42-20 devices are full frame devices, with 2048 imaging pixels in the spectral direction and 1024 pixels in the spatial direction. In addition, in the serial register between the imaging pixels and each amplifier there are an additional 50 pixels which are covered with Aluminium and are not sensitive to light but can be used for calibration purposes. In total therefore, there are 2148 pixels in the serial register;
- Backthinned to maximise quantum efficiency;
- Three phase clocking with minimum row shift ~8µs and minimum pixel shift ~2µs (TBC);
- Used in MPP mode;
- There are two read out ports, one at each end of the readout registers. Charge will be clocked down rows in the spatial direction and read out in the spectral direction.

3.2 Basic design principles

Figure one shows a schematic design for the CCD ROE. The ROE will be sent values of key parameters (such as integration time) by the Instrument Control Unit (ICU). These values will be stored in the registers in the ROE, and used by the ROE to control the CCD operation.

The default integration mode of operation for the ROE will be to free run with a 100% duty cycle. The ROE will clock out and read the CCD every ten seconds, and then output the data to the ICU. The default integration mode means that, should command links be lost from the ICU, image data would still be available from the Camera. In the normal integration mode, an integration will be started by the ROE "flushing" the CCD a number of times to remove the current charge in the CCD. At the end of the integration period the ICU will command the ROE to begin clocking out of data, which is then be read by the ICU. The ROE will indicate when the end of frame is reached.

A range of ROE functionality (defined below), such as windowing, will be available using values uploaded into the ROE registers by the ICU during the integration period.

The key components of the design are as follows (described in more detail in section 4):

- Focal Plane array (FPA) - the FPA itself shall be placed at the EIS focal plane and shall contain the two CCD detectors. It may also contain both the pre-amps to amplify the signals measured at the output sources of each CCD amplifier and the level shifters which will level shift the clock pulses to the appropriate levels for the CCD. Alternatively, both the amplification of the CCD output source and the level shifting may be contained within the main ROE box which will connect to the FPA via a short (<100mm) length of flexi;
- bias supplies - to generate the required voltage levels for the CCDs;
- clock generators - to generate the appropriate logic clock pulse sequences ;
- binning shall be implemented in the spatial and spectral direction;
- one variable width window shall be provided for each half of the CCD;

- boot up circuitry - various values (TBD) shall be stored in the ROE registers such that, after a power up, the ROE will be in a known default state;
- CCD signals shall be measured via a correlated double sampler with subsequent analogue to digital conversion. This digital data shall then be sent to the ICU (the manner in which the data is sent to the ICU is still TBD);
- the ROE shall receive and act upon the appropriate register values (these values are defined in appendix one) and suitable status commands (such as start of integration) from the ICU. The manner of data transmission to the ICU is still TBD, however, timelines showing the sequence in which data is transmitted (and the ROE operates) is shown in figure two, and discussed in more detail below in section 4;
- the ROE shall send the digitised CCD data to the ICU as a digitised stream of data packets. It shall also send over relevant status information and housekeeping information, either amongst the data packet stream, or as a separate lower speed housekeeping link - the exact interface is still TBD;

  If no signal is received by the ROE from the ICU after a defined period of time (time period to be TBD) then the ROE shall switch to a 'free running' mode in which the camera will integrate for 10 seconds, before reading out the CCD and sending the image data to the ICU via the high speed link. The camera shall then begin the next integration/data read cycle. The use of a free running mode ensures that images would be available from the camera even if the ICU were not able to command the camera (for example, after loss of the low speed link);
- the ICU shall power down either the FPA, the ROE or the entire camera unit;
- test ports shall be available to allow testing of the ROE via an external EGSE, without using the ICU. In addition, several test points may be provided to allow the analogue CCD signal to be viewed from each port without the need to download images via the ICU;

3.3 Date transfer modes

3.3.1 Data format protocols

The data format is still TBD. At the current stage of the design, the likely format is for each digitised pixel to be streamed out of the ROE as a 16 bit word, consisting of 14 bits of information containing the digitised values from the A/D, and 2 bits identifying the origin (which CCD and which output amplifier).

3.3.2 Data output rate

This is still TBD. The Video data rate from the camera must be sufficient to enable the camera to be operated at its maximum cadence rate. For example, using four output ports, at 500kpixels/s, and using 14 bit A-D conversion with a 16 bit word and CCD port labels, would lead to a maximum data rate of 32 Mbits/s.

4 ROE specification

The detailed specifications for the ROE are listed bellow. These requirements are summarised and tabulated in table one. The pinout voltages required for the CCD are shown in table two.

4.1 ROE circuitry

4.1.1 Master Reset

It shall be possible to send a master reset to the ROE (4.1.1a), initialising the registers to the default values and returning the ROE to the free running mode.

4.1.2 Clock speed - TBD

4.1.3 ADC Resolution

The ADC resolution shall be 14 bit (4.1.3a). *The amplifier gain will be set at 12 electrons/DN (4.1.3b)* to leave 'spare' dynamic range available to cope with issues such as upward drift of offset bias over time.

4.1.4 Time for correlated double sample

Due to the photoelectric effect, an incident photon will be converted into a number of electrons. At the short wavelength range (170Å) one photon will generate about 20 electrons, and at the long wavelength range (290Å) one photon will generate about 12 electrons.

Thus, an amplifier gain of 12 electrons/DN is equivalent to a gain of approximately one photon/DN at the EIS wavelengths. A noise performance of ± 1 DN should be acceptable. Consequently, a slow clamp and sample time during correlated double sampling to minimise the on-chip read out noise is not necessary.

A clamp and sample rate sufficient to allow a readout rate of 2µs per pixel shall be adopted (4.1.4a). Using the figures in the Marconi 42 series data sheet, such a time will correspond to a rms read noise of about 6 electrons.

4.1.5 Dump charge using the dump drain/flush the CCD

It shall be possible to quickly dump charge from the CCD using the dump drain provided (4.1.5a).

It shall be possible to dump a single line of the CCD; multiple lines; or the entire CCD (4.1.5b).

A dump drain is provided with the 42 series CCDs allowing unwanted rows to be quickly clocked out of the CCD. A row is clocked into the serial register. If the dump gate is held high (+12V ±2V) then the charge will drift out of the serial register and into the dump drain. During the dump cycle, the "integration" electrodes of the readout registers (e.g RØ1 and RØ2) remain high, and the low electrode (e.g RØ3) remains low.

It shall be possible, at least for testing purposes, to not flush the CCD before each image (4.1.5c).

4.1.6 Read out to left/right amplifier or both simultaneously

For each CCD, **it shall be possible to specify whether the charge read out is to be from the left hand amplifier, the right hand amplifier, or both (4.1.6a).**

Typical register values which could be used to implement such a scheme are shown below:

0	0	Clock each half towards its own amplifier.
0	1	Clock both halves of CCD towards left amplifier.
1	0	Clock both halves of CCD towards right amplifier.
1	1	Charge Injection (TBD) - defined in 5.2.5

4.1.7 Variation in clocking rates, imaging phase and voltages

The following functionality shall be provided. Default values shall be used, but it shall be possible to alter these values for testing, or to set new defaults during flight:

- **Vary the rate at which the CCD is clocked out (TBC) (4.1.7a).**
- **(TBC) Vary the phases which are held high during integration (e.g IO1 or IO1/IO2) (4.1.7b)**;
- Varying voltages to remove potential radiation induced flat band voltage shifts. - **vary the voltage of V_{RD}, V_{OD} and V_{SS} over a range of 4 volts with 16 steps (i.e, ¼ volt) being used (4.1.7c)**.

Typical register values which could be used to implement such a scheme are shown below:

Integration phases - default value is 0 and 1 high (integration under 1 and 2).

bit no	Sets
0	Int_phase1
1	Int_phase2
2	Int_phase3

4.1.8 CCD/ROE power down

It shall be possible to completely power down the CCD, the ROE or both (4.1.8a)(for example, in a high cosmic ray flux, see 5.2.7 below).

4.2 Imaging modes

4.2.1 Window read out

It shall be possible to select a known area of the image in the form of a rectangular window (4.2.1a) (i.e region of interest). Charge from pixels prior to the read out window, and after the read out window, do not need to be read and can be quickly dumped.

Four windows shall be available, one for each output port (4.2.1b).

Windows shall be of any width (within the half of the CCD) but both windows on the CCD must be the same height (4.2.1c).

Note: it must be remembered that there are 50 non imaging pixels at both ends of the serial register. That is, to read out pixel 0 from the image, it will first be necessary to read out 50 pixels from the serial register.

It is possible to clock out the CCD from the left hand output port and/or the right hand output port. It is suggested that Window 1 corresponds to clocking out in the left port, window 2 in the right port. If readout from one port only is required, then one of either window can be selected as appropriate.

4.2.2 Binning in the serial and parallel registers

Hardware binning in both the spatial and spectral directions shall be available (4.2.2a).

Binning can be implemented in the spatial direction by clocking more than one row into the serial register before clocking out the charge in the serial register.

Binning in the spectral direction can be implemented by suppressing the reset pulse to the output amplifier when clocking a charge packet onto the amplifier.

The serial register in the Marconi 42-20 CCD chip allows up to 300k electrons to be binned in before non-linearity appears. This value should be sufficient for EIS. Consequently, it will not be necessary to adopt the low responsivity mode that is available. Thus, the sensitivity of the output gates (OG1 and OG2) does not need to be adjustable as the maximum number of electrons that may be binned into the serial readout register is limited by the dynamic range of the CCD.

During testing, it would be useful to be able to bin all the charge into any number of pixels deemed appropriate. Therefore, two registers could be used to hold the X and Y bin values, but **each binning register shall be 12 bits long (4.2.2b)** to allow binning of all pixels (including overclocked pixels) into one pixel.

4.2.3 Integration time

The default mode of operation shall be for the ROE to be free running, clocking out the CCD every ten seconds (4.2.3a).

It shall also be possible to control the integration time by sending commands from the ICU (4.2.3b).

At the start of an integration, the ROE shall perform a number of "flush" commands (4.2.3c).

Once the flush is completed, the ROE shall set the voltages on each imaging electrode phase (4.2.3d) to allow charge to be accumulated.

During the integration period, the ROE shall update any new register values which have been sent from the ICU (4.2.3e).

The ICU shall terminate the integration by sending a 'start clocking' command. **When it receives this command, the ROE shall begin clocking out the CCD (4.2.3f),** implementing any binning and windowing specified in the registers **and shall indicate the end of frame (4.2.3g).**

If the ROE does not receive a command from the ICU after TBD time interval, it shall revert to the default free running mode (4.2.3h).

4.2.4 Overclocking

The 42 series CCDs have 50 'lead-in' pixels at each end of the serial register which have to be clocked through the output amplifier before the first pixels containing image information are measured. **It shall be possible to obtain additional, non-imaging pixels by 'overclocking' pixels within each row (4.2.4a)** (i.e. continuing to clock and read charge in the output amplifier after the last lead in pixel has been read). As 12 bits are available to specify the row coordinates there will be a maximum of 4096-2048-100 = 1898 pixels available for overclocking (at most about 50 would be expected to be used).

In addition **it shall also be possible to overclock the CCD in the spatial direction (4.2.4 b)** (i.e, creating "virtual" rows). Thus, the register value which contains the number of rows to clock must be large enough to handle 2048 rows.

The default value shall be no overclocking during an image, but it is anticipated that a number of test macros will be developed with varying values of overclocking.

4.2.5 Charge injection capability

(TBD) Charge shall be injected through one of the CCD readout amplifiers to minimise potential CTI (4.2.5a). The operating points from one (or both) of the readout amplifiers shall be changed such that small amounts of charge can now be injected into the serial register. This charge is then clocked through the serial (i.e readout) registers to provide a "thin zero" and fill a majority of the available charge traps. A row of data is clocked into the serial register as usual, and this charge can then be read out in the conventional way, but with potentially a much lower CTI as the majority of traps will still be "full" from the initial charge injection. A method of implementing charge injection is discussed in reference [2].

4.2.6 Cosmic ray monitoring

It shall be possible to monitor the cosmic ray flux within the CCD camera (4.2.6a). If the instantaneous cosmic ray flux at the CCD becomes to high, it may be advantageous to cease the measurement sequence and power down the CCD (TBD). A small 100x100 pixel area of the CCD which is not illuminated by the spectrometer should be monitored and an image downloaded every TBD seconds (or each frame, which-ever is the shorter period). The count rate detected within this area shall be compared with a pre-determined value stored in the EIS ICU and if the count rate is above this value, a terminate measurement and suspend sequence command should be issued.

The area to be monitored will be set after launch. How this is best implemented is TBD and will be discussed with the SOT and SXT instrument teams.

4.2.7 Test Ports

Test ports shall be available to allow testing of the ROE via an external EGSE (4.2.7a), without using the ICU. In addition, several test points may be provided to allow the analogue CCD signal to be viewed from each port without the need to download images via the ICU.

4.2.8 Stim Patterns

i **It shall be possible to inject a known image pattern into the CCD (4.2.8a)**, so that this image can then be clocked out to determine how the image may be degraded by the readout process;

ii **A stim generator shall be built into the ROE logic (4.2.8b)** to allow precise identification of specific pixels

4.3 Calibration modes

Calibration modes shall be available. They will consist of a number of macros which will enable a range of measurement sequences. These are the requirements for potential CCD calibration modes:

1. access to the "raw" image -i.e the digitised pixel values;
2. access to a number of calibration modes, defined below.

4.3.1 Dark Current

It is assumed that the cooling of the CCD will be sufficient to make dark current a minimal problem. However, periodic dark current measurements will still be required.

Any periodic measurement of dark current should produce a map of the variation of dark current to correct for hot and flickering pixels. Periodic monitoring will be necessary to ensure no drift (and if there is, to monitor this drift).

4.3.1.1 Frequency of measurement - TBD

4.3.1.1 Measurement method -

i. Close shutter

ii. Integrate

iii. download data - from either the entire chip or, for n lines onto which the spectra are normally imaged

iv. repeat

4.3.2 Flat Field

There are two options for flat fielding:

a. open the shutter, and defocus the grating to provide a flat field source for the CCD;

b. close the shutter, and project light onto the shutter via a calibration diode (blue light with the same absorption depth as the EIS wavelengths ?)

4.3.2.1 Frequency of measurement - TBD

4.3.2.2 Measurement method

i. Close shutter then switch on calibration diode OR open shutter and defocus grating

ii. Integrate

i. download data - from either the entire chip or, just the 120 lines onto which the spectra are normally imaged

ii. repeat

iii. turn off diode

4.3.3 Overscan

overscanning pixels is not a calibration mode in itself, but will be used in the following calibration modes.

a. CTI determination

b. bias determination

c. read noise determination

4.3.3.1 Frequency of measurement - whenever the calibrations below are required

4.3.3.2 Measurement sequence

i. follow the sequence for the required calibration mode

ii. clock out the CCD, but clock out n additional lines in the vertical direction

4.4.4 CTI

It will be necessary to monitor the CTI periodically as part of the camera's standard operating procedures. These measurements will require the following modes:

4.4.4.1 Use of an Fe55 source

i. the shutter is closed

ii. the "shutter" for the Fe55 source is opened and exposed for n seconds

iii. the CCD is clocked out, possibly including overscanned pixels

4.4.4.2 flat fielding

either one of the two flat fielding techniques are used in which the CCD is clocked out:

i. as for a "normal" image measurement

ii. also reading out the overscanned pixels

4.4.5 Read out noise

This measurement would be required very rarely. The value of the read out noise could be obtained by making a number of flat fielding measurements at different intensities. The slope of the ratio of signal (in DN) versus variance of the signal (in DN) will yield the readout amplifier gain, and the intercept with the signal axis will yield the read out noise.

4.4.5.1 Frequency of measurement - TBD

4.4.5.2 Measurement sequence

i. follow the sequence for either one of the flat fielding modes

ii. clock out the CCD

4.4.6 Bias Value

The bias value corresponds to the value which would be obtained for "zero" photons. The bias level could either be obtained by:

a. integrating for zero seconds

b. measuring the charge collected in the overscan pixels (as long as no CTI is present)

4.4.6.1 Frequency of measurement - TBD

4.4.6.2 Measurement sequence

i. integrate for zero seconds

ii. clock out the CCD with overscan

4.5 Other modes

4.5.1 Thermal control

A combination of a passive radiator and resistive heating must be provided to keep the operating temperature of the CCD within its defined limits (TBD) and to permit a heating of the CCD (TBC) to allow some annealing of possible radiation induced damage and to drive off any surface contaminants (TBC).

Minimum temperature required : -65°C (TBC)

Maximum temperature required : +30°C (TBC)

Range within temperature must be maintained: 2°C (TBC)

Maximum allowable heating (or cooling rate): 10°C/minute

4.6 Ground Test Modes

A number of additional modes will be required for ground based testing, but which will not be required for actual operation.

4.6.1 TBD

5 Detailed Design

5.1 CCD bias voltages

CCD bias voltages for each pin are described in appendix 2.

5.2 Power Distribution

5.2.1 Requirements

The CCD and ROE can be powered off completely

6 EMC requirements

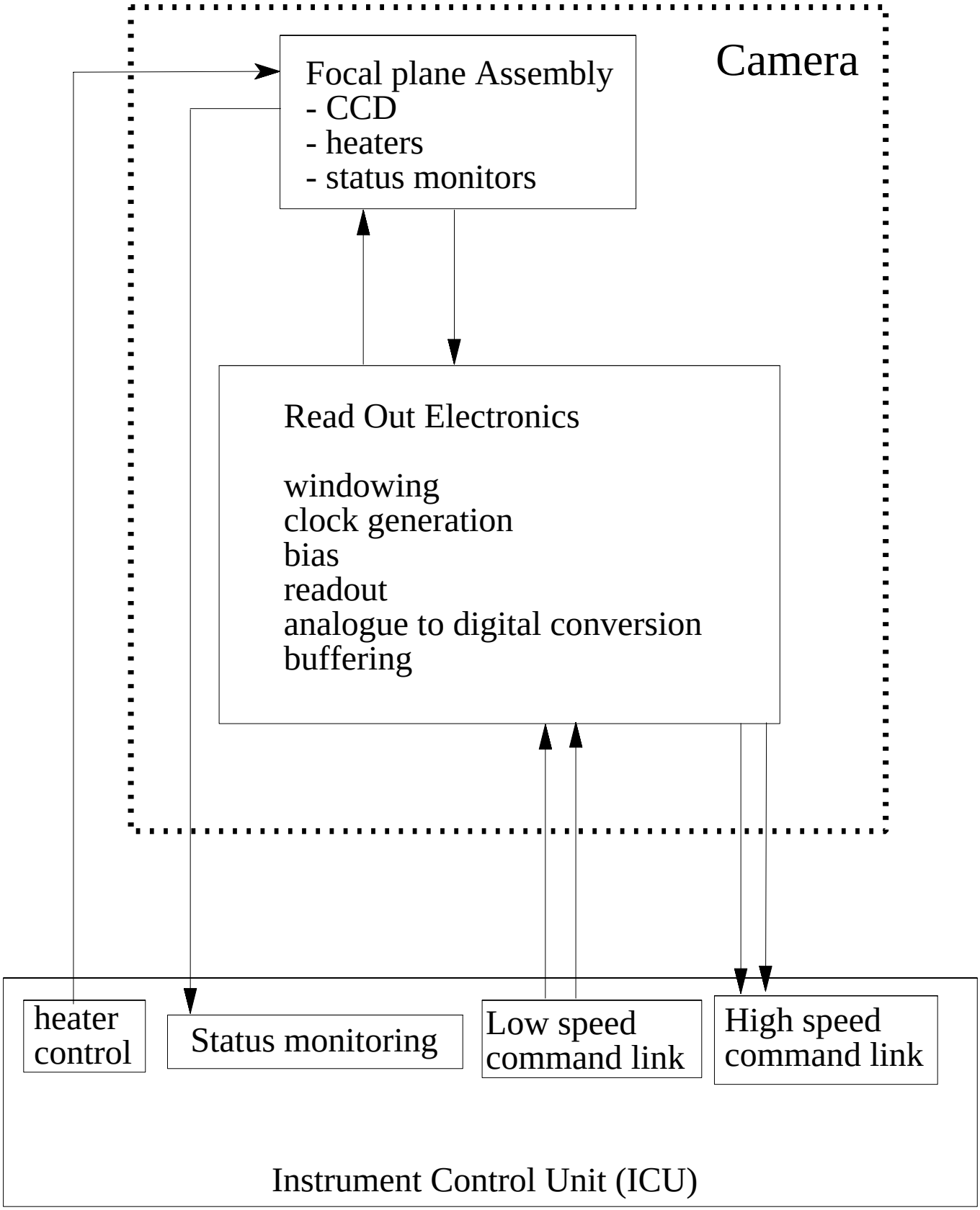
Camera
Focal plane Assembly
- CCD
- heaters
- status monitors
Read Out Electronics
windowing
clock generation
bias
readout
analogue to digital conversion
buffering
heater control
Status monitoring
Low speed command link
High speed command link
Instrument Control Unit (ICU)

Figure one

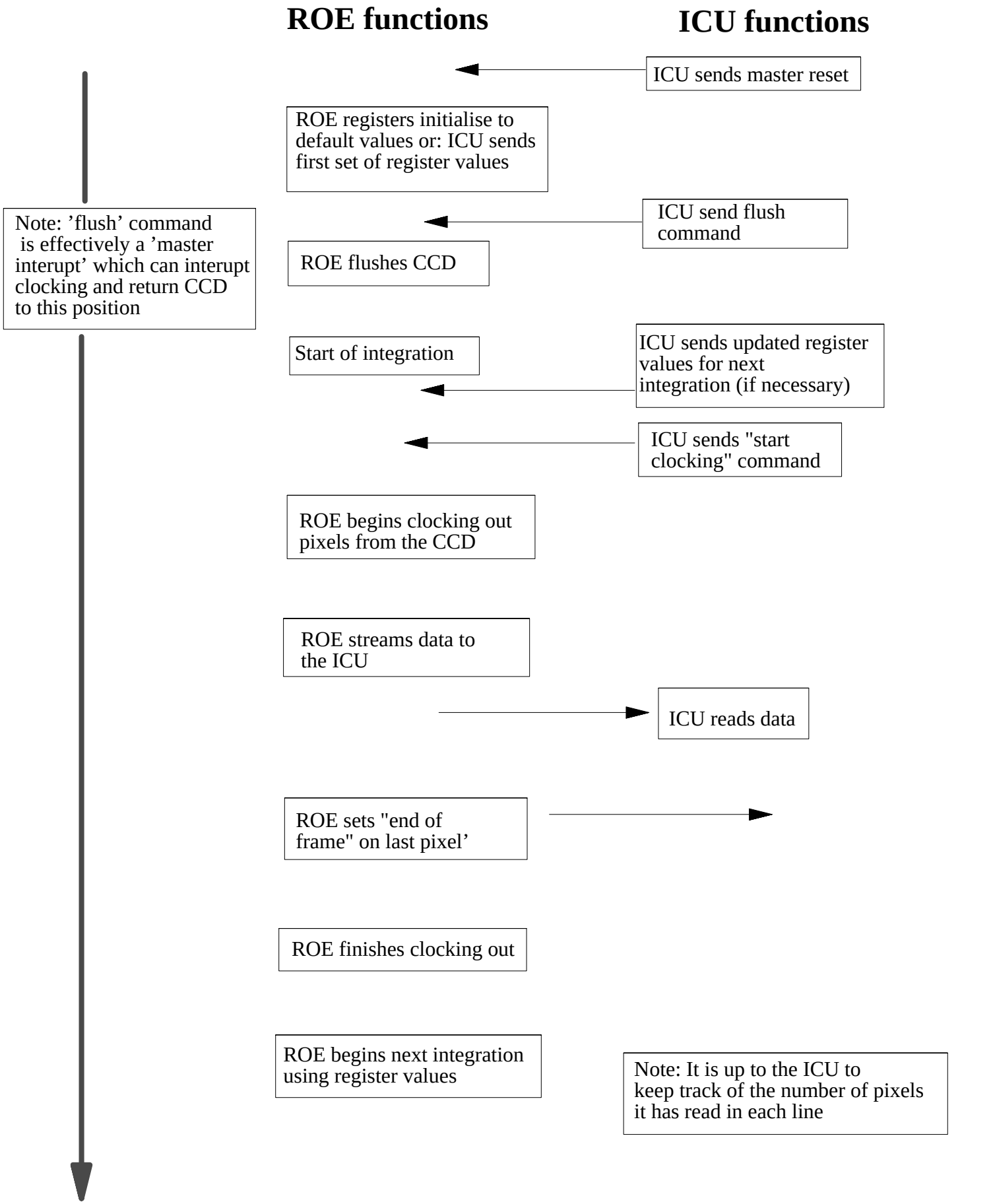

Figure two

Author : Chris McFee
Title : Integration command sequence
Date : 31 March 2000
Version : 2.1

		Summary of ROE design requirements
4.1.1		**Master reset**
	a	It shall be possible to send a master reset to the ROE
4.1.2		**Clock speed**
4.1.3		**ADC resolution**
	a	The ADC resolution shall be 14 bit
	b	The amplifier will be set at 12 electrons/DN
4.1.4		**Clamp and sample time**
	a	The clamp and sample time shall be sufficient to allow each pixel
		to be read in 2µs
4.1.5		**Charge dumping**
	a	It shall be possible to quickly dump charge from the CCD from the CCD
		using the dump drain provided
	b	It shall be possible to dump single lines, multiple lines, or the entire CCD
	c	It shalll be possible, for testing purposes, to not flush the CCD before an image
4.1.6		**Readout amplifier**
	a	It shall be possible to specify whether charge is read out from the left
		hand amplifier, the right hand amplifier, or both
4.1.7		**Varying clocking rates, voltages and phase during flight**
	a	vary the rate at which the CCD is clocked out (TBC)
	b	vary the phases which are held high during integration (TBC)
	c	vary Vod, Vss and Vss over a range of 4 volts over 16 steps
4.1.8		**CCD/ROE power down**
	a	It shall be possible to completely power down either the CCD, or the ROE, or both
4.2.1		**Window read out**
	a	It shall be possible to select a known area of the image in the form of a
		rectangular window
	b	Four windows shall be available, one for each output port
	c	Windows shall be of any width but both windows in each CCD must be the same height
4.2.2		**Binning**
	a	Hardware binning in both the spatial and spectral directions shall be available
	b	Each binning register shall be 12 bits long
4.2.3		**Integration**
	a	The default mode for the ROE shall be free running, clocking out the
		ccd every 10 seconds
	b	It shall also be possible to control the integration time by sending commands
		from the ICU
	c	At the start of integration, the ROE shall perform a number of
		flush" commands
	d	The ROE shall set the voltages on each imaging electrode phase
	e	During integration, the ROE shall update any new register values which have
		been sent by the ICU
	f	On receipt of a "start clocking" command, the ROE shall begin clocking
		out the CCD
	g	The CCD shall indicate end of frame
	h	If the ROE does not receive a command from the ICU after TBD time interval
		it shall revert to the default free running mode
4.2.4		**Overclocking**
	a	It shall be possible to obtain additional, non-imaging pixels by overclocking
		pixels within each row
	b	it shall be possible to overclock the CCD in the spatial direction
4.2.5		**Charge injection**
	a	It shall be possible to inject charge through a readout amplifier
		to minimise potential CTI problems
4.2.6		**Cosmic ray monitoring**

	a	It shall be possible to monitor the cosmic ray flux within the CCD camera
4.2.7		**Test ports**
	a	Test ports shall be provided to allow testing of the ROE via an external EGSE
4.2.8		**Stim Pattern**
	a	It shall be possible to inject a known image pattern onto the CCD
	b	A stim generator shall allow precise indentification of specific pixels

Table one

Provisional 42-20 pin out voltages

Chris McFee
10/4/2000

42 pin out voltages and maximum ratings
Actual pin out numbers will vary. This table is based on the nominal 42-20 pin outs presented by EEV in December 1999

pin no	name	L/R	min volts	typical volts	max volts	maximum ratin	comments
1	SS		0	9	10		
2							
3							
4							
5	Io3		8	12	14	±20	
6	Io1		8	12	14	±20	
7	Io3		8	12	14	±20	
8	SS		0	9.5	10		
9	OS	L	3-5 below OD			-0.3 to 25	
10	OD	L	27	29	31	-0.3 to 35	
11	DD		22	24	26	-0.3 to 30	
12	RD	L	15	17	19	-0.3 to 25	
13	SS		0	9.5	10		
14	OG2	L	see com				OG1 +1 for normal low noise, 20V for binning
15	OG1	L	1	2	3		
16	oSW	L	9	12	15	±20	clock as Ro3
17	DG		-	0	-	±20	for charge dumping, pulse 12 +/- 2V
18	oR	L	9	12	15	±20	
19	Ro2	L	9	12	15	±20	
20	R01	L	9	12	15	±20	
21	R03		9	12	15	±20	
22	Ro1	R	9	12	15	±20	

23	Ro2	R	9	12	15	±20				
24	oR	R	9	12	15	±20				
25	DG		-	0	-	±20	for charge dumping, pulse 12 +/- 2V			
26	oSW	R	9	12	15	±20	clock as Ro3			
27	OG1	R	1	2	3					
28	OG2	R	see com				OG1 +1 for normal low noise, 20V for binning			
29	SS		0	9.5	10					
30	RD	R	15	17	19	-0.3 to 25				
31	DD		22	24	26	-0.3 to 30				
32	OD	R	27	29	31	-0.3 to 35				
33	OS	R	3-5 below OD			-0.3 to 25				
34	SS		0	9.5	10					
35	Io2		8	12	14	±20				
36	Io1		8	12	14	±20				
37	Io3		8	12	14	±20				
38										
39										
40										
41	SS		0	9.5	10					
		Table two								