Solar B - EIS

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Solar B EIS ROE Digital PCB Design Description Iss. 1

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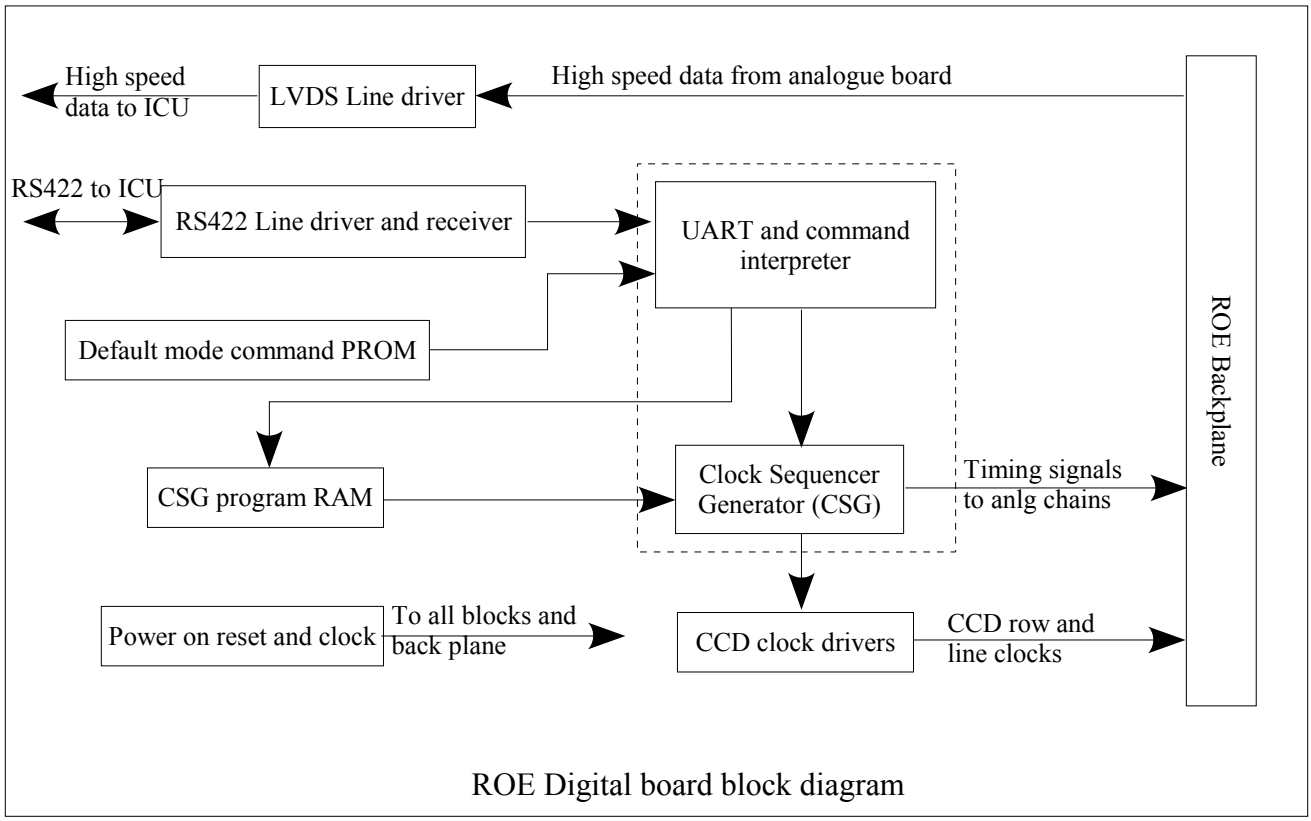
MSSL/SLB-EIS/SP001.03; 4 July 2000; "EIS CCD Camera - System Requirements"
A5725 016 EIS ROE Digital PCB Schematic, Issues 1 (PM) and 2 (PFM and FM)

Contents

1 Introduction

The EIS ROE digital PCB is responsible the following functions:
It provides the Command, Status and Science data interfaces to the ICU.
It provides the timing signals required by the analogue PCB and the CCDs.
It controls the bias voltages for the two CCDs.
It controls the 'nap' mode of the ADCs on the power and analogue PCBs.
It interprets and acts upon commands from the ICU.
It provides status information to the ICU when requested.
It provides the ICU with end of CSG sequence information.
It provides the 13.5V CCD clock drivers.



ROE Digital board block diagram

2 Power on reset

When powered up or reset the ROE enters 'default mode', which causes the camera to perform a sequence that will allow the instrument to read out the CCD if the command link has failed. This default mode is also very useful for testing the camera when it is not integrated in a full system. This read out sequence consists of a CCD flush, followed by an eight second integration time and, finally, the CCDs are read out twice with a 1024x512 frame size. The sequence then repeats. The initial fifty covered pixels on each line are discarded. The two read outs are separated by a gap of between 12ms, this is to give the ICU time to switch between buffers.
The default mode is stored as a series of commands in a PROM. These comprise: a command to set up the analogue electronics in a mode that is acceptable and a series of commands to program the CSG. The default values of the analogue parameters will not be known until tests with real CCDs have been completed.

The power on reset is also supplied to the Actel on the analogue PCB. This just resets the high speed link, sets the bias voltages to 'middle' levels and enables read out of all four CCD ports. When default mode starts running the bias settings are changed to the values store in the EPROM.

A hard reset command is available to allow the ICU to force the ROE back into default mode.

3 Electrical interfaces

3.1 Outputs from the digital PCB

Signal Name	*Type*	*Comments*
ROE Back-plane outputs		
A(5:0)	Digital bus 5V	Address bus for the analogue PCB
D(7:0)	Digital bus 5V	Data bus bi-directional
HK_MUX_SEL(6:0)	Digital bus 5V	House keeping analogue multiplexer select bits
HK_CONV_START_N	Digital 5V	House keeping ADC convert start signal
HK_SHUT_DOWN_N	Digital 5V	House keeping ADC nap mode signal
HK_OE_N	Digital 5V	House keeping ADC output enable
SYS_CLOCK	Digital 5V	32MHz system clock
SYS_RESET_N	Digital 5V	Main system reset
WR_EN	Digital 5V	Write signal to the analogue PCBs control registers etc
RD_EN	Digital 5V	Read-back from analogue Actel's registers
CONVST_N	Digital 5V	Science ADC convert signal
CLAMP_N	Digital 5V	CDS clamp signal
ISOLATE	Digital 5V	Anlg chain isolate signal side
SHUT_DOWN_N	Digital 5V	Used to put the science ADCs into nap mode
STIMR (Formerly STIMBRIGHT)	Digital 5V	Drives the stims to the analogue chains for CCDs A and B, right hand sides
STIML (Formerly STIMDARK)	Digital 5V	Drives the stims to the analogue chains for CCDs A and B, left hand side
EOS	Digital 5V	Indicates to the high speed link transmitter that this is an end of frame
I1A	13.5V	CCD A line clock phase 1
I2A	13.5V	CCD A line clock phase 2
I3A	13.5V	CCD A line clock phase 3
R1LA	13.5V/0.8V	CCD A pixel clock phase 1 LH side
R2LA	13.5V/0.8V	CCD A pixel clock phase 2 LH side
R3A	13.5V/0.8V	CCD A pixel clock phase 3 both sides
SWLA	13.5V/0.8V	CCD A summing well LH side

Signal Name	*Type*	*Comments*
RA	13.5V	CCD A reset signal
R1RA	13.5V/0.8V	CCD A pixel clock phase 1 RH side
R2RA	13.5V/0.8V	CCD A pixel clock phase 2 RH side
SWRA	13.5V/0.8V	CCD A summing well RH side
DGA	13.5V	CCD A dump gate
I1B	13.5V	CCD B line clock phase 1
I2B	13.5V	CCD B line clock phase 2
I3B	13.5V	CCD B line clock phase 3
R1LB	13.5V/0.8V	CCD B pixel clock phase 1 LH side
R2LB	13.5V/0.8V	CCD B pixel clock phase 2 LH side
R3B	13.5V/0.8V	CCD B pixel clock phase 3 both sides
SWLB	13.5V/0.8V	CCD B summing well LH side
RB	13.5V	CCD B reset signal
R1RB	13.5V/0.8V	CCD B pixel clock phase 1 RH side
R2RB	13.5V/0.8V	CCD B pixel clock phase 2 RH side
SWRB	13.5V/0.8V	CCD B summing well RH side
DGB	13.5V	CCD B dump gate
-10VA	Power	-10V power for the anlg switches in analogue chains for CCD A
-10VB	Power	-10V power for the anlg switches in analogue chains for CCD B
ROE Connector Outputs		
SCIENCE_DATA_STROBE+	LVDS	Serial data strobe to the ICU
SCIENCE_DATA_STROBE-	LVDS	Serial data strobe to the ICU
SCIENCE_DATA+	LVDS	Serial data to the ICU
SCIENCE_DATA-	LVDS	Serial data to the ICU
STATUS_LINK+	RS422	Status link serial i/f to the ICU
STATUS_LINK-	RS422	Status link serial i/f to the ICU

3.2 Inputs to the digital PCB

Signal name	*Type*	*Comments*
ROE Back-plane inputs		
HK_DATA_RDY	Digital 5V	The PSU PCB analogue to digital converter has finished
+13.5VD2	Power	Horizontal and vertical clock driver supply, CCDA
+13.5VD3	Power	Horizontal and vertical clock driver supply, CCDB
+5V1	Power	VCC for the 5V logic
+2V55	Power	2.55V power for the Actel core voltage
+14V5	Power	Voltage to drive charge pump for -10V
AGND	Power	Analogue ground for the CCD drivers
GND	Power	Digital ground
0V (+14V5 Return)	Power	Charge pump supply return

Signal name	*Type*	*Comments*
ROE Connector inputs		
COMMAND+	RS422	Command serial link from the ICU
COMMAND-	RS422	Command serial link from the ICU

4 Command interface

General

The command link sends commands to the ROE from the ICU at a fixed rate of 9600 bits per second (baud). The interface is a simple asynchronous protocol similar to RS232. It provides no hardware handshaking, so flow control may be provided by a command and acknowledge mechanism using the status link. Since such a handshake is not mandatory the ROE receiving system is capable of processing the incoming commands at an average rate greater than one byte per 1ms.
All commands are atomic and each unique type of command is always the same length, different types of commands have different lengths.
There is no true hardware error detection or correction.
No commands sent to the ROE are considered to be dangerous to the instrument or the satellite.

Physical layer definition

The physical layer defines the signalling levels, timing, connector pin out, cable requirements and maximum permissible bit error rates (BERs) of the links.
The link operates at 9600 bits per second.
The ICU sends sent one start bit, eight bits of data and one stop bit. The start bit is one complete bit time long and has a logical value of '0'. The stop bit is also one full bit time long and has a logical value of '1'. When the links are quiet the signalling level is a logical '1'.
The signalling levels on the links is differential RS422.
The cable environment is such that reflections and similar disturbances do not cause the links to exceed the permissible BER (TBD).
The connector pin out is defined in the Solar B EIS Pin out List.

Character layer definition

The character layer defines the content and meaning of characters and messages sent on the links. The following commands are used by the ICU to control the ROE:

CMD ID 1st Byte	**Name**	**No. of bytes**	**Description**
0x40	Reset	1	Performs a hard reset. Returns the ROE to default mode. All previously programmed parameters are lost. This command can not be executed until command 0x41 (Exit default) has been executed)
0x41	Exit default	1	Exit default mode, enter idle state. This command enables ICU control of the camera. No other commands will be processed or acknowledged until this command has been sent
0x42	Start CSG	2	Perform one CCD flush or read out. The second byte contains the six bit block ID for the CSG pattern. MSBs unused
0x43	Dump CSG	4	Dump the CSG RAM contents Byte 2 is the block select, Bits 0 - 5: CSG register block 0 to 63 Bit 6: Unused Bit 7: The pattern/program RAM selector Byte 3: The RAM page base address field, 5 LSBs Byte 4: The Address 6 LSBs bits 6 and 7 unused

CMD ID **1st Byte**	**Name**	**No. of bytes**	**Description**
0x44	Program CSG Windows	5	Set single byte entry in CSG program or pattern space, usually used to set up windows without reprogramming an entire CSG pattern or program block Byte 2 is the block select, Bits 0 - 5: CSG register block 0 to 63 Bit 6: Unused Bit 7: The pattern/program RAM selector Byte 3: The RAM page base address field, 5 LSBs Byte 4: The bottom 6 address bits Byte 5: Byte set up data

CMD ID 1st Byte	Name	No. of bytes	Description
0x45	Setup AE	9	Program the analogue PCB Byte 2 Bias register 1 Bits 3 - 0: CCDA VOD Bits 7 - 4: CCDB VOD Byte 3 Bias register 2 Bits 3 - 0: CCDA VRD Bits 7 - 4: CCDB VRD Byte 4 Bias register 3 Bits 3 - 0: CCDA VSS Bits 7 - 4: CCDB VSS Byte 5 Control register 1 Bit 1,0: Unused Bit 2 CCDA VOG2 "1" Normal, "0" Low gain Bit 3: CCDB VOG2 "1" Normal, "0" Low gain Bit 4: stim_isolate_n "0" isolates the stim generators Bit 5: self_test_n, "0" Use internal data pattern generator Bit 6: Running "1" Enables the internal pattern generator. "0" Disables the internal pattern generator. Bit 7: reserved Byte 6 Control register 2 Bit 0: "1" Analogue chain CCDA R enable Bit 1: "1" Analogue chain CCDA L enable Bit 2: "1" Analogue chain CCDB R enable Bit 3: "1" Analogue chain CCDB L enable Bit 4 - 7: Reserved Bytes 7 - 8: Reserved for additional registers Byte 9 SEU counter (1) Read only, reported by the Analogue param dump command
0x46	Set up CSG	67	Program the CSG Byte 2 is the block select, Bits 0 - 5: CSG register block 0 to 63 Bit 6: Unused Bit 7: The pattern/program RAM selector Byte 3: The RAM page base address field, 5 LSBs Bytes 4 - 67: 64 bytes of CSG register setup data

CMD ID 1st Byte	Name	No. of bytes	Description
0x47	HK request	2	Request an HK parameter. Byte 2 is the HK parameter Id, listed in table 2
0x48	CSG Sig	2	This generates a CSG signal, SIG0 or SIG1. Byte 2 bit 0 indicates which signal, remaining bits unused. Details for the use of these signals are contained in the CSG description section
0x49	Dump AE parameter	2	Reads back one of the analogue electronics parameters programmed by command 0x45. Second byte is the number of the parameter 0 to 7, reading bytes 2 to 9 of the command 0x45 respectively
0x4A- F	Spare		

Notes:
There is no "soft reset command" (which leaves parameters unchanged).
(1) This byte is not available on the PM ROE

Error Detection
The receiver implements a limited amount of error detection: the first byte is checked for a valid Command ID (0x40 to 0x49) any other value will cause a NACK to be sent on the status link; the receiver also counts the number of bytes following a valid header byte and if too few are received (this is determined if there a a gap of more than 250ms), will respond with an NACK. See below.

5 The Status Interface

The status link is used for returning HK requests, ROE read out status information and providing register read back to the ICU. It runs at a fixed rate of 9600 baud. The interface is a simple asynchronous protocol similar to RS232. It provides no hardware handshaking, so flow control can only be provided by a status and acknowledge mechanism using the Command Link. All status messages are atomic and two bytes long. Data buffering is provided at the ICU receiver using a FIFO buffer 4 bytes deep.

Physical layer definition
The link physical characteristics are identical to the Command Link.

Character layer definition
The character layer defines the messages from the ROE to the ICU:

ROE HK/Status list

Message ID 1st Byte	Name	No. of bytes	Description
0x03	ACK or Error	2	Second byte indicates the nature of the error. A second byte of 0x00 is ACK. A second byte of 0x01 is an unrecognised command header A second byte of 0xFF is a time-out error. The commands that generate an ACK are: 0x41, 0x42, 0x44, 0x45, 0x46, 0x48
0x0C	End of sequence	2	Indicates a sequence has finished, (or rather the CSG program has set one of the end of flush or end of read out bits). Byte 2 is the block number at the time the CSG set one of the bits.
0x30	Dump CSG	2	Dump the CSG RAM contents. Byte 2 is the requested byte.
0xC0	HK and AE dump	2	Read out HK or AE parameter. Byte 2 is the requested byte.

ROE HK values

HK ID	Name	Sig. Bits	Type	Calib. Const.
0	+5VD	8	Voltage	

HK ID	Name	Sig. Bits	Type	Calib. Const.
1	+2.5VD	8	Voltage	
2	+5VA_A	8	Voltage	
3	+5VA_B	8	Voltage	
4	-5VA_A	8	Voltage	
5	-5VA_B	8	Voltage	
6	+36V_A	8	Voltage	
7	+36V_B	8	Voltage	
8	+12V_A	8	Voltage	
9	+12V_B	8	Voltage	
A	CCDA VOD	8	Voltage	
B	CCDA VRD	8	Voltage	
C	CCDA VSS	8	Voltage	
D	CCDB VOD	8	Voltage	
E	CCDB VRD	8	Voltage	
F	CCDB VSS	8	Voltage	
10	+5VD	8	Current	
11	+2.5VD	8	Current	
12	+5VA_A	8	Current	
13	+5VA_B	8	Current	
14	-5VA_A	8	Current	
15	-5VA_B	8	Current	
16	+36V_A	8	Current	
17	+36V_B	8	Current	
18	+12V_A	8	Current	
19	+12V_B	8	Current	
1A	UPPER TEMP	8	TEMPERATURE	
1B	LOWER TEMP	8	TEMPERATURE	
1C	-10V_A	8	Voltage	
1D	-10V_B	8	Voltage	
1E	SPARE MON	8	--	
1F	SPARE MON	8	--	
20 - 3F	RESERVED	8	--	

6 Science interface

Introduction
The link supplies CCD readout data in serial form that is used to build a CCD image in ICU RAM. The ICU discards data that are not required by the scientists and passes the remainder to the spacecraft for forwarding to the ground.
The maximum science data rate is a 14 bit word from each side of each CCD every 2us. This corresponds to a rate of 28Mbits per second. A 2 bit header is required to identify the CCD source of each data word, so the total data rate is 32Mbits per second.
Block error detection is provided (a block is an entire CCD read out frame).
Soft error recovery is provided on a block basis.
Bit or character error detection is not available.
No error correction, either forward or backward, is provided.

Physical layer definition
The physical layer defines the signalling levels, coding, connector pin out, cable requirements and maximum permissible bit error rates (BERs) of the science link. Connector pin-out and cabling are defined in the EIS Instrument cabling requirements.

The link operates at 32Mbits per second.
The signalling levels on the link is differential LVDS. (Ref 1.)
The cable environment is such that reflections and other disturbances do not cause the link to exceed the permissible BER.

The link comprise two differential signals known as data and strobe.
Data is sent serially on the data signal pair and the link operates in such a fashion that if two consecutive bits of data are the same the strobe changes from its current state to the other.
While the link has no data to transmit the data and strobe both remain in the state defined by the last bit sent.
The receiving end of the link uses the data and strobe to recover a 16MHz clock. This clock stops toggling when there is no data. It is recovered by taking the exclusive OR of the data and strobe.
The maximum BER shall be set at 3.5x10E-10 errors per bit (TBD). Calculated from an average of one bit error per 1000 frames. This BER shall be formally defined so that the supporting digital logic guarantees an SEU rate less than one tenth of this (TBD).

Character layer definition

The character layer defines the format of data that is transferred on the link.

The active link sends only two types of character:
1. Science data characters. These are 16 bits long and comprise a pair of CCD node identification bits and fourteen data bits. The first bit sent is the CCD ID ('0' is CCD A, '1' is CCD B), the second bit is the node ID ('0' is the left hand side of the CCD and '1' is the right hand side of the CCD), the third is the most significant bit of the data, the last (sixteenth bit) sent is the least significant bit of the data.
   The transmitter sends the pixels in a fixed order, the first sent has the node ID and CCD ID bits set to "00", the second "01", the third "10" and the fourth "11".
2. End of frame character. This character is eight bits long and is used to indicate to the ICU that the last science data character sent was the final character of a frame. This character has only one valid bit pattern, and is always 0xCC.

Transaction layer definition.
The transaction layer defines how the two ends use the data (or lack of it) on the link to determine how these data are to be used and how to recover from soft errors.

During nominal link operation the transmitting end sends science data characters with no gap between them exceeding the receiver's Period of Silence (defined below). The maximum gap between data words determines the maximum horizontal binning factor that can be supported. The receiver uses the two most significant bits of each science data character to determine where each data word originated. At the end of a line there is a gap of approximately 200us (TBC) before the first character of the next line is transmitted. The Period of Silence is greater than the maximum line shift time that is likely to be used. This determines the maximum vertical binning factor.

At the end of a frame the transmitter shall leave a gap of one Period of Silence after sending one, and only one, eight bit end of frame character.

The receiver is able to receive, process and store data from one entire CCD through one single CCD port, i.e. potentially twice as much data from a frame with the two most significant bits the same as would be the case when reading a CCD out of two ports. If one CCD is being read out of a single port then the other CCD must also be read out of a single port, but this need not be the same port.

Definition:
The link uses the absence of data (known as a Period of Silence) as a error detection mechanism in the following way:
There are two Periods of Silence defined: the Sending Period of Silence (10ms) and: the Receiving Period of silence (9.9us). The Receiving Period of silence is shorter than the Sending one so that we can guarantee that the transmitter does not time out before the receiver. This could arise because the two ends are synchronised to different clocks. In the following the two different Periods of Silence are implied by which end is doing the measuring.

If the receiver's incoming science data character is unfinished after a Period of Silence the data in the current frame was corrupt. This can arise from two situations:
1. The sending end of the link has lost synchronisation in its transmission. In this case the recovered 16MHz clock may be left high during the Period of Silence.
2. The receiving end has lost synchronisation with the incoming link. In this case the recovered clock will always be left low.

The receiving end recovers unilaterally from condition '2' by resetting its bit counter(s) to zero after its Period of Silence has passed, this will allow the link to recover synchronisation at the start of the next frame. If situation '1' has occurred the receiving end will be unable to recover alone.

The sending end also uses its Period of Silence to recover from '1'. After a Period of Silence, it then (and only then) sets the data and strobe to a zero condition, to return the recovered clock to zero, and resets all of its bit counters. The transmitter will start to send data from the next frame when commanded to by the ICU. This is could cause the receiver to detect the change of clock state during transmitter reset and assume it is the start of the first character of a new frame. For this reason the ICU

should not restart an ROE read out until a further period of silence if it detects an error on the link. If there is no permanent damage to the link, synchronisation will be restored at the start of the next frame.

A valid end of frame is indicated to the to the receiver by an end of frame character followed by a Period of Silence. This prevents the receiver from responding to a corrupted data word that is a truncated eight bit science word. The parsing of the data value after the Period of Silence will help to eliminate the possibility of a corrupt, truncated, eight bit character at the end of a frame (because the requirement of a Period of Silence would still be met). The only situation that could give rise to an erroneous end of frame detection at the receiver is if the link generates an erroneous, 8 bit, truncated, 0xCC character at the end of a CCD frame, followed by an erroneous Period of Silence. The chance of this is very low. If the receiver receives an otherwise valid end of frame that has a value different from 0xCC it will probably assume that there was a soft error in the end of frame byte. The end of frame is indicated to the ICU, and the received value placed in a status register which the ICU may read. The ensuing behaviour of the ICU is beyond the scope of this document, but see the previous paragraph.

7 Clock Sequence Generator (CSG) Specification and Description

The CSG design is simplified by making the assumption that the clocks to the CCDs (row or line) should not change state during the analogue to digital conversion of any video information. This requirement is placed upon the EIS ROE system by noise requirements.
The consequences of this assumption are that:

1. The two halves of a CCD must have identical H/W windows, otherwise the row and line clocks from one side of the CCD will be running when video is being digitised from the other side.
2. The windowing on each CCD must be identical, this follows from '1'.
3. In the event of a failure of one node of one CCD the other CCD must be read out in the same fashion, i.e. from one node, although it may be the opposite node.

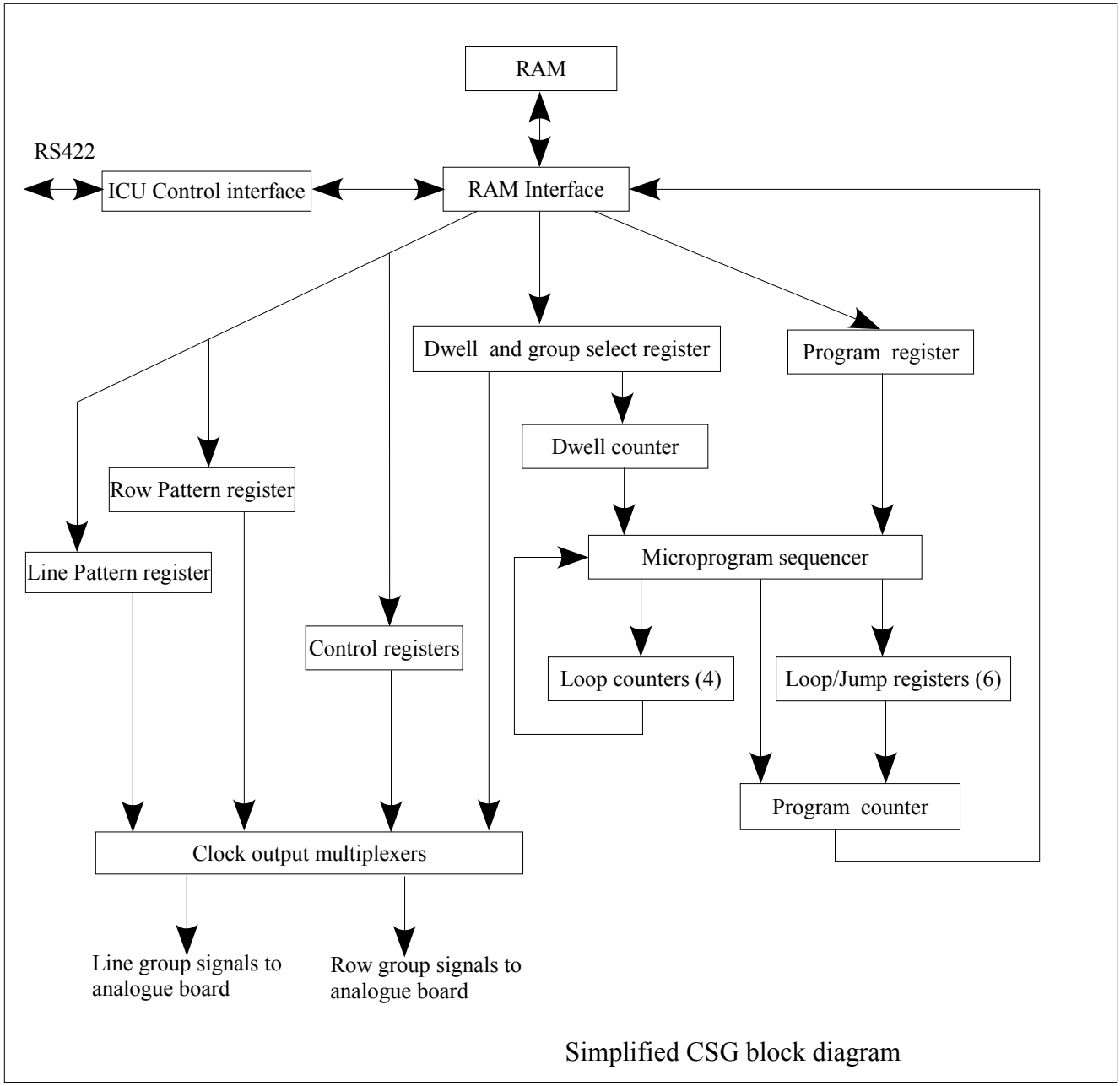
This means that the CSG MUST clock both CCDs in the same way all of the time, therefore only one CSG is required.

General description.
The CSG design is very generic. It is a single Actel with two RAMs to store clock patterns and control sequences for generating the CCD and analogue clocks. The clock sequencer only uses about 20% of an RT54SX32S Actel FPGA.
The design is based on a micro-program sequencer which reads simple programs from one RAM bank and reads clock patterns from another, it updates output clock signals with the values read from the RAMs when required. The current design divides the output signals into two groups, with a maximum of eleven independent signals in each group. The CSG can change the value of signals in one group or the other at any one time, but not both at once. Therefore the current CSG design can generate twenty-two different outputs from these two groups. The EIS ROE requires more outputs, but because the two CCDs are clocked synchronously, they are not all independent and control registers are used to demultiplex single pattern bits onto multiple identical outputs.
It is capable of running one of sixty-four sequences that may be stored at any one time in its RAM. It is envisaged that only two or three of them: frame flush, readout or dithering, will be used under normal circumstances. After completing a sequence it idles (Halted) until instructed to do otherwise.
After a reset it idles until a start sequence command is received. Responsibility for performing the default mode read out sequence rests with the ROE controller section of this PCB, it issues the start sequence commands.
The EIS design uses two 128K banks of memory, both 8 bits wide, one to store predominantly patterns and one to store predominantly sequence programming information. The RAMs are broken up into blocks of 2K bytes each. When the CSG receives a START command it reads one byte from each of the RAMs, taking two clock cycles. It assembles the two bytes into one sixteen bit word, the top four or five bits defining the function of the remaining bits. The lower bits can be control register information, or a pattern to be output. Four 32MHz clock cycles are used per instruction, giving a maximum output update rate of 8MHz, 125ns, so a typical 2us read out pixel requires 16 updates.

A START command is received by the CSG as a write from the ICU command interface to a control register (START register). A six bit value is written to this register, reflecting the block (sequence number) out of which data will be read for the next readout. The CSG will start running from location 0 in the selected block.
To run a series of different patterns, e.g. a flush followed by a readout, the individual programs would be loaded into different memory blocks, then the controller would write the first block ID into the START register, wait until the sequence has finished then write the second block number to the START register. All other control information is contained within the sequence program.

Program counter.
This is used to generate the addresses of instructions and data fetched from RAM. It is incremented after every instruction, and is loaded by START, JBOS or DJNZ instructions (see instruction set summary below).

Looping.
The sequencer has a number of loop counters which can be used for repetitive operations, such as reading out a row of 512 pixels, the pattern and sequence for a pixel need be written only once and surrounded by a loop. These loops can be nested, for example, for multiple rows. There are four loop counters implemented. There are two instructions used for looping: LOADn



Simplified CSG block diagram

and DJNZn. The first instruction loads the number of times the loop is to be executed into the relevant loop counter, and loads the address of the next instruction into the relevant return address register. The second (Decrement and Jump if Not Zero) updates the pattern output register, decrements the relevant loop counter and if the count has not finished, it jumps to the address in the relevant return address register. A loop count of zero is not supported, a loop count of one will execute a loop a single time.

Dwell Control register.
Dwell counter register and update group register. The time taken to execute an instruction (ie progress to output update) can be controlled, so each instruction can take a programmed length of time to run. This allows slower operations, such as line shifts, to be programmed without using very long sequences of instructions or big loops. One bit in this register controls which update group is being used (see pattern registers below). The dwell control register is eleven bits long, bits 9 to 0 are the number of 125ns time slices the next instructions will take to execute, bit 10 selects the update group ('0' for the pixel group and '1' the line group). A value of '0' written to the 10 lsbs causes the execution time to be 125ns, a value of '1': 250ns, so the delay is strictly the number of additional states to be used (so execution time is 125ns x (n +1) where 'n' is the value in the 10 lsbs). The delay relates only to instructions that update the outputs. Instructions can be programmed to have an execution time up to 128 us.

Once an update group has been selected that group remains active for all subsequent instructions, the other outputs do not change state, until another LDWL instruction is executed.

Pattern registers

These are two eleven bit registers that store the current state of the twenty-two independent output bits. The micro-program sequencer updates one of these registers when an instruction includes a pattern update field. These registers are named the 'row' and 'line' group registers and are defined as follows:

Row Group

D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
chrg_sync	stim_left	stim_right	clamp_n	convst_n	isolate	sw_n	rr_n	r3_n	r2_n	r1_n
-10V charge drive signal (1)	Test stim left	Test stim right	CDS clamp signal	ADC start conversion	ADC input isolate	CCD summing well	CCD Reset	CCD Rphi3	CCD Rphi2	CCD Rphi1

Line Group

D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
lspare1	chrg_pmp	15v_on	flush_cmplt	rdout_cmplt	eos	shutdown	dg_n	i3_n	i2_n	i1_n
	-10V charge pump enable (1)	+15V ON increases line clocks to 15V (1)	Send end of flush to status link	Send end of readout to status link	Send end of sequence to HS link	Power down science ADCs	CCD dump gate	CCD Iphi3	CCD Iphi2	CCD Iphil

Notes:
(1) These outputs are not available on the PM version of the ROE. Changing these bits has no effect on the PM.
A '1' written to the chrg_pmp bit causes the charge pump for the -10V supplies to be timed by the csg. A '0' causes the charge pump to by driven by a free running 500kHz oscillator.
While the csg is in control of the charge pump it is driven by chrg_sync.
The 15v_on bit is used on the PFM to drive a constant current source for a test led. It is unused on other models.

The load dwell counter instruction (see above) includes a bit (10) that selects which of these two group registers will be updated.

Stopping continuous operation.
The CSG can execute a program indefinitely, by using an absolute jump back to the beginning of a sequence. The absolute jump instruction has a break facility, the ICU can send a 'generate signal 0' or 'generate signal 1' command. After one of these commands has been received the micro-program sequencer will break out from the loop when it reaches a JBOSn instruction (Jump or Break On Signal n). This instruction should be the last in a loop and the instruction following it will be executed after a signal has been received. The destination of a JBOSn jump is determined by loading the jump registers 0 or 1, this is done just before the infinite loop is entered (LDSIGnJ instruction).

Micro-program sequencer instructions.
The instructions for the sequencer are sixteen bits. These instructions are composed of two fields: a four or five bit instruction field, and a twelve or eleven bit data field.

The instructions break into three types:

Prog Bits 7- 4	Prog/Pattern bits 3 - 0	Pattern bits 7 - 0	Details
Control type			
0000	0, Pattern	Pattern	HALT, Stops the sequencer. The CSG will restart using the same or another program when the ICU sends a start CSG command. A pattern is output.
0000	1, Data	Data	CTRLREG0, load control reg. 0 with data, no output change
0001	0, Data	Data	CTRLREG1, load control reg. 1 with data, no output change
0001	1, Data	Data	CTRLREG2, load control reg. 2 with data, no output change
0010	0, Data	Data	CTRLREG3, load control reg. 3 with data, no output change
0010	1, Data	Data	CTRLREG4, load control reg. 4 with data, no output change
0011	0, Data	Data	LDWL load dwell reg. with data, set update group (bit 10), no output. Any instructions (that update the outputs) following this will take the amount of time specified by the 10 lsbs of this register to execute.
0011	1, -	-	Spare
General type			
0100	-	-	Spare
0101	0, Unused	Unused	LDSIG0J, load the JBOS0 jump address register with the address of the next instruction, ie, the program counter (PC)
0101	1, Unused	Unused	LDSIG1J, load the JBOS1 jump address register with the address of the next instruction
0110	-	-	Spare
0111	-	-	Spare
Loop/pattern type			
1000	Data	Data	LOAD0 counter 0 from prog bits 3 - 0 and pattern RAM 7 - 0 and load the counter 0 address register with the PC
1001	Data	Data	LOAD1 counter 1 from prog bits 3 - 0 and pattern RAM 7 - 0 and load the counter 1 address register with the PC
1010	Data	Data	LOAD2 counter 2 from prog bits 3 - 0 and pattern RAM 7 - 0 and load the counter 2 address register with the PC
1011	Data	Data	LOAD3 counter 3 from prog bits 3 - 0 and pattern RAM 7 - 0 and load the counter 3 address register with the PC
1100	0, Pattern	Pattern	DJNZ0 counter 0 to address register 0, output pattern
1100	1, Pattern	Pattern	DJNZ1 counter 1 to address register 1, output pattern
1101	0, Pattern	Pattern	DJNZ2 counter 2 to address register 2, output pattern
1101	1, Pattern	Pattern	DJNZ3 counter 3 to address register 3, output pattern
1110	0, Pattern	Pattern	JBOS0, to absolute address in jump reg. or break on sig0, output pattern
1110	1, Pattern	Pattern	JBOS1, to absolute address in jump reg. or break on sig1, output pattern
1111	0, -	-	Spare
1111	1, Pattern	Pattern	NOP, output pattern and go on to next instruction

Details of the output de-multiplexers used for EIS

The EIS CSG is customised from the generic solution by the output de-multiplexers. The control of these is absolutely crucial to the functionality of the ROE. The five control registers that perform this are programmed from the program and pattern

memories by the control register load commands in the instruction table above. The control function and default value of the registers are defined below. The control registers can be considered to be concatenated into a single register 55 bits wide. This is how the functionality is described. The reset state is suitable for 'normal' operation, ie reading out of all 4 nodes, both CCDs active.

Bit number	Ctrl reg. and bits	Reset (default state)	Output controlled (Signal, side, CCD)	Description
1,0	Reg0 1 & 0	0,1	R1, r, a	Selects the source for R phi 1, side right, CCD a "00" output '0' "01" output R1 of row group "10" output R2 of row group "11" output '1'
3,2	Reg0 3 & 2	0,1	R1, l, a	Ditto for R phi 1, side left, CCD a
5,4	Reg0 5 & 4	0,1	R1, r, b	Ditto for R phi 1, side right, CCD b
7,6	Reg0 7 & 6	0,1	R1, l, b	Ditto for R phi 1, side left, CCD b
9,8	Reg0 9 & 8	1,0	R2, r, a	Ditto for R phi 2, side right, CCD a
11,10	Reg1,0 & Reg 0, 10	1,0	R2, l, a	Ditto for R phi 2, side left, CCD a
13,12	Reg1 2 & 1	1,0	R2, r, b	Ditto for R phi 2, side right, CCD b
15,14	Reg1 4 & 3	1,0	R2, l, b	Ditto for R phi 2, side left, CCD b
17,16	Reg1 6 & 5	0,1	R3, -, a	Selects the source for R phi 3, CCD a "00" output '0' "01" output R3 of row group "10" output R3 of row group "11" output '1'
19,18	Reg1 8 & 7	0,1	R3, -, b	Ditto for R phi 3, CCD b
21,20	Reg1 10 & 9	0,1	RR, -, a	Selects the source for R phi Reset, CCD a "00" output '0' "01" output RR of row group "10" output RR of row group "11" output '1'
23,22	Reg2 1 & 0	0,1	RR, -, b	Ditto for R phi Reset CCD b

Bit number	Ctrl reg. and bits	Reset (default state)	Output controlled (Signal, side, CCD)	Description
25,24	Reg2 3 & 2	0,1	SW, -, a	Selects the source for R phi SW, CCD a See note 1 "00" output '0' "01" output SW of row group "10" output SW of row group "11" output '1'
27,26	Reg2 5 & 4	0,1	SW, -, b	Ditto for R phi SW, CCD b
32 to 28	Reg2 10 to 6			Spare
34,33	Reg3 1 & 0	0,1	I1, - , a	Selects the source for I phi 1, CCD a "00" output '0' "01" output I1 of line group "10" output I1 of line group "11" output '1'
36,35	Reg3 3 & 2	0,1	I1, -, b	Ditto for I phi 1, CCD b
38,37	Reg3 5 & 4	0,1	I2, - , a	Selects the source for I phi 2, CCD a "00" output '0' "01" output I2 of line group "10" output I2 of line group "11" output '1'
40,39	Reg3 7 & 6	0,1	I2, -, b	Ditto for I phi 2, CCD b
42,41	Reg3 9 & 8	0,1	I3, - , a	Selects the source for I phi 3, CCD a "00" output '0' "01" output I3 of line group "10" output I3 of line group "11" output '1'
44,43	Reg4, 0 & Reg3, 10	0,1	I3, -, b	Ditto for I phi 3, CCD b
46,45	Reg4 2 & 1	0,1	DG, - , a	Selects the source for Dump Gate, CCD a "00" output '0' "01" output DG of line group "10" output DG of line group "11" output '1'
48,47	Reg4 4 & 3	0,1	DG, -, b	Ditto for Dump gate, CCD b

Note 1 - The CCDs have independent summing wells on each side of the CCD. All four are routed on the back plane. However, since Rphi3 is common to both sides, there is no point keeping the summing wells separate in the de-multiplexers.

Software development tools
An assembly language version of a clock sequence can be passed through the CSG assembler, the output of which can be converted to commands for the ICU or Motorola hex for loading into an EPROM through other software tools. In addition, a macro replacement assembler is available that makes writing CSG programs a little easier. This takes a slightly more intuitive language. The advantages of this are that pieces of code that are re-usable can be defined once in a macro and instantiated into the main code blocks as required, the language is easier to understand and only changes to outputs need be defined.
The macro assembler commands map 1:1 to low level assembler instructions as follows:

Macro Command	Discription	Low level equivalent
ASSIGN outputs	'outputs' from the CSG after DWELL	NOP
BREAK_ON_SIG0 outputs	loop back to last LOOP_UNTIL_SIG0, unless sig 0 is high,'outputs' from the CSG after DWELL	JBOS0
BREAK_ON_SIG1 outputs	loop back to last LOOP_UNTIL_SIG1, unless sig 1 is high, 'outputs' from the CSG after DWELL	JBOS1
CTRLREG0 data	'data' for ctrl register 0, 11 bits	CTRLREG0
CTRLREG1 data	'data' for ctrl register 0, 11 bits	CTRLREG1
CTRLREG2 data	'data' for ctrl register 0, 11 bits	CTRLREG2
CTRLREG3 data	'data' for ctrl register 0, 11 bits	CTRLREG3
CTRLREG4 data	'data' for ctrl register 0, 11 bits	CTRLREG4
GROUP LINE,DWELL = m	0 <= m < 1024 (m+1) x 125ns = dwell time	LDWL
GROUP ROW,DWELL = m	0 <= m < 1024 (m+1) x 125ns = dwell time	LDWL
HALT outputs	'outputs' from the CSG after DWELL	HALT
LOOP0 n	0 < n < 4096 n is the number of times to loop	LOAD0
LOOP1 n	0 < n < 4096 n is the number of times to loop	LOAD1
LOOP2 n	0 < n < 4096 n is the number of times to loop	LOAD2
LOOP3 n	0 < n < 4096 n is the number of times to loop	LOAD3
LOOP_UNTIL_SIG0	start of infinite loop until sig 0	LDSIG0J
LOOP_UNTIL_SIG1	start of infinite loop until sig 1	LDSIG1J
NEXT0 outputs	loop back to last loop0, 'outputs' from the CSG after DWELL	DJNZ0
NEXT1 outputs	loop back to last loop1, 'outputs' from the CSG after DWELL	DJNZ1
NEXT2 outputs	loop back to last loop2, 'outputs' from the CSG after DWELL	DJNZ2
NEXT3 outputs	loop back to last loop3, 'outputs' from the CSG after DWELL	DJNZ3

Clock sequences can be written in either language, however the macro replacement language is probably easier to maintain.

The CSG RAM interface
The RAM interface on the FM version of the ROE has in-built hardware error detection and correction. It is transparent to the ICU. When a data byte is written to the program or pattern RAM four bits of check data are also written. These form a simple hamming code that allow detection and correction of SEUs. If an error is detected it is corrected and the SEU counter is incremented. If the error is detected by the CSGs command interpreter it pauses the clock sequence to allow the corrected data to be written back to RAM. Two bit errors are detected, but may not be correctly interpreted as two bit errors, and may be mistaken for a single bit error in another position. There is no way of determining if this has occurred, so if a non-zero SEU count is noted it is probably better to re-load the clock sequence at the next opportunity.

This is not supported on the PM ROE.

Details of the stim pattern implemented in block six of the flight PROM
This pattern consists of a series of vertical and horizontal stripes symmetrical about the vertical centres of the two CCDs. The pattern is superimposed on any image that is acquired at the time, so the shutter is best left closed when running this block. The CCDs appear to be 2048x512 pixels.
Each side of the CCD takes the following form:
243 lines of:
- 1 dark pixel
- 1 light pixel
- 1 dark pixel
- 1 light pixel
- 2 dark pixels
- 2 light pixels
- 2 dark pixels

2 light pixels
4 dark pixels
4 light pixels
4 dark pixels
4 light pixels
8 dark pixels
8 light pixels
8 dark pixels
8 light pixels
16 dark pixels
16 light pixels
16 dark pixels
16 light pixels
32 dark pixels
32 light pixels
32 dark pixels
32 light pixels
64 dark pixels
64 light pixels
64 dark pixels
64 light pixels
128 dark pixels
128 light pixels
128 dark pixels
128 light pixels
1 dark pixel
1 light pixel
1 dark pixel
1 light pixel
15 dark lines
249 lines the same as the first 243
5 bright lines

Document end.