Photocopiers in space?

A proposal for a 6 Msps 14 bit 4 channel CCD Analogue Front End adaptable for Solar-B EIS flight hardware and SOT CCD qualification

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Contents

1 Requirements

There now exists a general requirement for a second generation MSSL Read Out Electronics (ROE) and adaptation of the INTEGRAL EGSE to follow the success of the INTEGRAL flight system, which was also used for the qualification of the SXI and EIS CCDs. This second generation ROE and EGSE must meet the Solar-B EIS flight hardware requirements, and could also be used for the higher speed read out requirements of the Solar-B SOT CCD qualification, and other possible future CCD programmes.

This document contains a proposal for a second generation CCD ROE to cater for read out speeds of up to 6 Msps at 14 bit resolution, and 15 Msps at 13 bits. The design uses high speed multichannel signal processors developed for colour photocopiers and high resolution cameras. We firstly review the immediate requirements for Solar-B EIS and SOT.

1.1 Solar-B EIS.

These are stated in MSSL/SLB-EIS/SP05 Design Requirements for the Solar-B EIS Read Out Electronics. The EIS camera has two CCD42-20 CCDs, both AIMO (MPP), 1024(V) x 2048(H), a total of 4 read out ports.
Photon shot noise ~12 e- rms
Required read out noise ~6 e- rms.
Pixel rate is 500 ksps.
A science requirement is an Analogue to Digital Converter (ADC) resolution of 14 bits at low illumination levels, though for photon counting14 bits over the entire dynamic range of the ADC is preferable.

1.2 Solar-B SOT Focal Plane Package (FPP)

The following summary of requirements is extracted from the minutes of the CDR for the CCDs, held at Marconi Applied Technology (MAT), 11-12 July 2000.
The SOT FPP contains three CCDs with read out noise required as follows:
CCD74 2048(H) x 1024 (V), 11 e- rms at 3 Msps
CCD75 1024(H) x 224(V), 11 e- rms at 3 Msps
CCD80 50(H) x 50(V), 9 e- rms at 2 Msps
ADC resolution 14 bits.

2 Space qualified parts

It is sometimes difficult to find parts which are suitable for the space environment, especially high speed analogue parts. Often the specifications of available space qualified parts conflict so far as space instrumentation is concerned, e.g. speed vs. power consumption and thermal dissipation, reliability and radiation tolerance vs. cost. The requirements of Solar B suffer from this problem, particularly concerning parts suitable for the Correlated Double Sampler (CDS) and the ADC.

3 Possible solutions

3.1 Sub-qualification of COTS.

There has been much discussion within ESA, NASA and the wider space industry about the use of Commercial Off-The-Shelf (COTS) parts for space flight, and there are arguments both for and against their potential use. A reasonable approach would be to work with a manufacturer of commercial parts to produce parts which meet subsets of standards for space use. Issues such as package hermeticity, cleanliness (outgassing), radiation tolerance and reliability need to be addressed. One manufacturer, Linear Technology Corp (LTC) has proposed a sub-qualification exercise, e.g. a repackaging of a plastic encapsulated ADC (LTC1419, 800 ksps 14 bit) with electrical parameters guaranteed for a subset of the total specification with a basic MIL-STD-883C

level B test flow. The matter of radiation tolerance would also need to be addressed. The over-riding issue for MSSL would most likely be one of cost, which might be mitigated in the case of a common parts procurement programme such as the one performed by ESA for INTEGRAL. A sub-qualification approach might be possible within the SOLAR-B consortium, but the general usefulness of a 800 kps 14 bit part is probably limited as far as the future requirements of MSSL are concerned. Far better to consider faster parts such as the one proposed in 3.3 below.

3.2 Space qualified ADCs in non-linear configuration

Dave Walton has suggested a brilliant idea for a dual-range ADC scheme whereby the lower end of the dynamic range is digitised to a finer resolution. For example, a 10 bit ADC could be used for the upper range and an 8 bit ADC for the lower range where the equivalent of14 bit resolution is required. This kind of approach is available on-chip in commercial compandor ICs used in digital voice communication systems. There are suitable space qualified standard ADC parts available, but power dissipation is still a general problem. There would also be a need to produce a monotonic transition between the coarse and fine ranges using external gain and offset trim resistors, and this might be difficult to guarantee over the life of the mission.

3.3 Commercial CCD/CIS Signal Processor (CSP)

I am aware of at least two semiconductor manufacturers which are now shipping in high volume complete analogue front end devices capable of high speed, multi-channel read out for CCDs and Contact Image Sensors (CIS). Target markets include high resolution colour photocopiers and high resolution imagers and vision systems. For example, the AD9814 CCD Signal Processor (CSP) from Analog Devices Inc (ADI) is a complete analogue signal processor on a chip. Features include a 3-channel architecture (RGB inputs) comprising 3 input clamps, 3 Correlated Double Samplers (CDS), 3 Programmable Gain Amplifiers (PGA), all multiplexed into one 14 bit ADC, with guaranteed performance from 0 to 70C of 6 Msps in multiplexed 3-channel and single channel modes. Total 28-SOIC package size over leads is only 18 mm x 10 mm, power consumption at 6 Msps is only 220 mW with a thermal resistance from junctions to case of only 23 °C/W. There is also a faster version of the device, the AD9822 which ADI claims will run at 15 Msps, but with reduced front end noise of 1.5 LSB rms, compared with 0.53 LSB rms in the AD9814. The effective number of bits of the AD9822 will therefore be ~13, as compared with ~13.5 for the AD9814.

4 Proposal for CSP solution for EIS.

The block diagram attached shows a minimal scheme consisting of four AD9814 CSP chips with all inputs and outputs isolated from neighbouring parts and with switchable power connections, providing true cold redundancy which is fail-safe. To meet the EIS flight requirements, all components used for isolation and power switching must be space qualified parts or else the cold redundancy concept falls apart or becomes too complicated to implement, and hence less reliable. One could imagine a much larger array of cold redundant CSP chips, but things could begin to get a bit silly!

In the minimal scheme any combination of CSPs may be powered at any one time. Normally only two CSPs are required to read out the 4 ports from the two CCDs. The CSPs are arranged in pairs, two per CCD, and normally only one is required to read out the 2 ports of each CCD. Should a CSP fail, then it is powered off and its inputs and outputs are isolated from the circuitry, and its cold redundant partner is brought into play. Only 2 analogue inputs of each CSP are used, the third is grounded.

The inputs are isolated by separate buffer amplifiers, which also have switched power for power saving. A combination of amplifier and analogue multiplexer could also be used.

To cater for faster read out rates, as in the case of qualification of the SOT CCDs, pixel rates of up to 3 Msps per channel are possible in the multiplexed 3 channel mode, or 6 Msps in single channel mode. Either mode could be used for SOT. Lockheed may also be interested in considering the CSP at for the Solar-B SOT flight ROE.

Pixel data emerges from the CSP chip in parallel byte format (R>G>B): R high byte (8 bits), R low byte (6 bits), G high byte, etc., with a pipeline delay of approximately 3 pixel clock periods. In the single channel case, only the selected channel is processed.

In the proposed scheme, the digital outputs and control inputs are isolated by an FPGA which must be capable of operating at the fastest possible rates, with internal propagation delays carefully controlled in the design. Such a device is the Actel 54SX16A, a rad hard device with cell-to-cell propagation delays in the range 0.1 to 1.2 ns for fan outs 3 or less. In the case where pixel rates of up to 6 Msps are required the serial data rate over the LVDS link is 6 x 16 = 96 Mbps (including a 2 bit overhead for the CCD port ID). The standard configuration for the EIS hardware is to combine the two right CCD ports into one serial stream, and similarly the two left ports, so the combined rate would be 192 Mbps over each LVDS link. While the LVDS concept is good for rates above this, it might be difficult to design data generation and capture hardware which will work at this speed, so a non-combined channel approach might be more sensible. Thus at the 3 Msps pixel rate the non-combined rate reduces to 48 Mbps per CCD port, which is closer to the design goal of 32 Mbps for the EIS flight LVDS links. This would enable the same ROE and EGSE hardware to be used for both EIS and SOT requirements. However, it might make sense to design the EGSE to cope with much faster rates for future projects.

5 Reliability

ADI publishes reliability reports for their products. Reliability Report no. FY99-1118 applies to the AD9814; the following is a summary of its contents.

5.1 0.6µm CMOS (C6) process

The AD9814 is fabricated in the 0.6 µm double polysilicon, double metal (DPDM) CMOS process (C6). The C6 process was qualified at ADI's Limerick, Ireland, wafer fab in 1996. During fiscal 1997, a total of 4,263,304 equivalent device-hours were accumulated on the C6 process with zero failures during life testing at 125C, 135C or 150C of 2946 normal production samples from 56 lots. The resulting calculated failure rate was 3 FIT (failures in 10^9 hours) when derated to 55C using the Arrhenius relation assuming an activation energy of 0.7eV and a chi-squared failure distribution with a 60% confidence level. It should be noted that these data and predictions are of course relevant to the silicon die only, not the packaged devices.

5.2 Package

The 28-SOIC package assembled at ADGT Philippines has been qualified. ADI claims that no significant reliability deficiencies have been identified with this package type through the original qualification or subsequent routine reliability evaluations. Tests include 1000 cycles Thermal Shock from –65C to +150C; 168 hrs Autoclave testing at 2.0 Bar, 121C, 100% rh; 1000 hrs Temperature-Humidity Bias (THB) at 85C and 85% rh; 3 cycles of Resistance to Solder Heat.

In addition to generic tests, there were specific tests on AD9814 devices from one wafer lot.

5.3 ESD

Human Body Model (1.5k•, 100 pF), highest pass ±4000V; Machine Model (1•, Cpkg), highest pass ±1500V. Positive and negative charges were applied to every individual pin to AVdd, AVss, DrVdd, DrVss; every individual I/O to the group of all other I/O pins.

5.4 Latch-up

Tested to JEDEC Std 78. Device powered at +3V, at 25C. Current pulses, ±150mA, 50µs risetime, 10ms duration, applied to each individual input and output pin. Test performed with all input pins at +3V, then all at GND. Similar tests performed with voltage pulses up to +5.5V.

6 Screening of parts for flight

The initial approach, as already discussed in para. 3.1, would be open a discussion with other potential users within the Solar-B consortium about a possible sub-qualification exercise, and with ADI. Regardless of the outcome of this, the following steps are proposed as a minimum screening requirement. This would include radiation testing, endurance testing and a benign burn-in of flight parts. We might also consider an SEM examination of several parts, and possibly a 100% PIND tests

of potential flight parts. All tests would be performed on samples of one batch out of which the flight devices are selected. This batch must be procured in a single time order by the selected distributor and having the same package date code. Without wafer traceability this is probably as close as we will get to the ideal. Of course, the package date codes will give no indication of the wafer source of each die.

There is no radiation data available from ADI for the AD9814. However, radiation test data from ADI's RadTest Service, which is not warranted, is available from tests performed by end users on similar devices fabricated in the CMOS processes. Further investigation is required in this area.

To overcome the problem of making electrical connection to the SOIC package, the burn-in of flight parts could be performed in situ on partially populated flight boards. This would provide a degree of confidence prior to thermal vacuum testing, which is expensive and often schedule critical. Final board assembly, board and unit level electrical testing and environmental tests would follow the burn in of partially populated boards.

A possible screening plan might look something like this (temperatures are derated from the ADI absolute max specs.):

Radiation total dose gamma	10, 20, 30, 40, 50, 75,100 kRad	14 pcs
Endurance	1000 hours +125C biased	10 pcs
Flight parts burn-in	72 hours +70C biased	16 pcs (4 PCBs)
Spare stock and attrition		60 pcs
Total single order qty		100 pcs

The current small volume price for the AD9814 is ~7 US$. The AD9822 is ~3 US$. One distributor, AVNET-MACRO, has quoted a similar numerical price in UK£, delivery 3-4 weeks.

7 Packaging for flight

In addition to the minimum screening proposed above, the parts would need to be suitably "packaged" on the PCBs. A suggested procedure could include some or all of the following:

7.1 Radiation shielding

Alternate high-/low-Z layers to minimise X-ray secondary emission, dense enough for total dose shielding as deemed necessary.

7.2 Hemiticity

Required to prevent moisture ingress prior to launch , and to prevent outgassing within the optical instrument. Suitable local conformal coating or potting could achieve this.

7.3 Heat sinking

May need some additional thermal paths to be added, though placement of devices close to wedge-lock card guides and conductive plane(s) may suffice. Approx 200mW per device, max of 2 powered at any one time. Thermal resistance junction-to-case of 23 °C/W is very low, so stress on chip will be minimal, producing a failure rate below the projected 3 FIT figure in the 55C reliability calculation.