Solar B – EIS

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SOLAR B –EIS Read-Out Electronics: Analogue Design Specification

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CHANGE RECORD

ISSUE	DATE	SECTIONS CHANGED	COMMENTS
01	02 Jul 2000	All new	
02	02 Jan 2001	6 & 7	Redistribution of functions on Analogue and Digital PCBs, update on selection of ADC.
03	16 Jul 2002	Title changed. All sections revised	Major revision to incorporate modifications tested on PM and design changes to FM. Includes the limitation of fault propagation from CCD A and CCD B and associated signal chains: separate CCD bias generators, stim circuitry and all power to pairs of signal chains. Clocking scheme and local test CSG defined.
04	08 Apr 2003	5.1.28 7.3.5 7.3.6 7.3.7 7.4.2 Fig. 8	Company name of CCD supplier was MAT, now E2V. Updates include change from 12V to 13.5V CCD clock voltage and detailed descriptions of analogue circuit design. Correction to fig. 8.

Contents

1 REFERENCE DOCUMENTS

RD1   MSSL/SLB-EIS/SP05 Design Requirements for Solar-B EIS Read-Out Electronics
RD2   MSSL/SLB-EIS/DD/004 CCD Camera Block Diagram
RD3   MSSL/SLB-EIS/DD/002 EIS Grounding Configuration
RD4   MSSL/SLB-EIS/DD/021 CCD Camera Grounding Configuration
RD5   MSSL/SLB-EIS/DD/022 ROE Analogue PCB Block Diagram
RD6   MSSL/SLB-EIS/SP/015 EIS Telecommanding Structure
RD7   A2/5275/004 Solar B EIS ROE Motherboard Pin Assignments
RD8   SLB-120 Solar-B Electrical Design Standard
RD9   MAT/DAS 547806 AT, CCD42-20 Interface Drawing (EIS)
RD10 MSSL/SLB-EIS/SP020.02 Electronic Component Specification

2 ABBREVIATIONS

ADC   Analogue to Digital Converter
ADI   Analog Devices Inc.
AGND   Analogue (Signal) Ground
AIMO   Advanced Inverted Mode Operation
CCD   Charge Coupled Device
CDS   Correlated Double Sampler
CGND   CCD Clock Ground
CSG   Clock Sequence Generator
CTE   Charge Transfer Efficiency
DG   CCD Dump Gate
DGND   Digital Ground
EIS   Extreme UV Imaging Spectrometer
FEE   Front End Electronics
FPA   Focal Plane Assembly
FPGA   Field Programmable Gate Array
H   Horizontal
ICU   Instrument Control Unit
Iø   Image (Vertical) Clock Phase (or Pulse)
L   Left (refers to left CCD port)
LSB   Least Significant Bit
LTC   Linear Technology Corporation
LVDS   Low Voltage Differential Signaling
MDM   Micro-D connector (with metal shell)
MHC   Mechanisms and Heaters Controller
MPP   Multi-Phase Pinned
MSB   Most Significant Bit
PGA   Programmable-Gain Amplifier
øR   Reset Clock Phase (or Pulse)
øSW   CCD Summing Well Clock Phase (or Pulse)
OS   CCD Output Source
PISO   Parallel In Serial Out register
R   Right (refers to right CCD port)
Rø   Read-Out Register (Horizontal) Clock Phase (or Pulse)
ROE   Read-Out Electronics
TBD   To Be Defined
V   Vertical
VOD   CCD bias Voltage at Output Drain
VOG   CCD bias Voltage at Output Gate
VRD   CCD bias Voltage at Reset Drain
VSS   CCD bias Voltage at Substrate

3 INTRODUCTION

The major science goals of the Solar-B mission are as follows: to determine the mechanisms responsible for heating the corona in active regions and the quiet Sun, to determine the mechanisms responsible for transient phenomena, such as flares and coronal mass ejections, and to investigate the processes responsible for energy transfer from photosphere to the corona. The instrument payload consists of the Solar Optical Telescope (SOT), X-ray Telescope (XRT), and EUV Imaging Spectrometer (EIS)

The EIS telescope is an off-axis paraboloid design, with multi-layer coated single mirror of focal length 1.9m and diameter 150 mm. EIS has a total length of 3 m. Multi-layer toroidal diffraction gratings disperse the spectrum via an entrance slit/slot onto two CCDs covering wavelength ranges 180 - 204 A and 250 - 280 A. Angular resolution is 2". Four slit/slot positions are available, currently a 1" slit and a 40" slot have been determined. Spectral/velocity resolution: 3km/s for Doppler velocities, 20 km/s for line widths. Temporal resolution in spectroscopy mode is < 1s in dynamic events, ~ 10 s in active regions. In imaging mode, monochromatic imaging of an active region (~ 4 x 4 arc min) in 3 s for dynamic events, 10 s otherwise. FOV: 360" x 512". EIS will provide monochromatic images of the transition region and corona at high cadence a slot. High spectral resolution images can be obtained by rastering with a slit.

The two CCDs are type CCD42-20, supplied by E2V, formally MAT and EEV. The devices are back-thinned, operate in full-frame mode, size 1024(V) x 2048(H) pixels, with read-out out ports at the right and left ends of the read-out register. Pixel resolution is 13.5 x 13.5 μm. The CCDs are fabricated for Asymmetrical Inverted Mode Operation (AIMO), i.e. Multi-Phase Pinned (MPP). This allows low dark current levels to be achieved without excessive cooling; for EIS the goal is –40 C. The CCD42-20 has 50 dummy pixels at either end of its read-out register. On-chip horizontal binning is achieveable by use of a summing well electrode at each end. A single dump gate allows the CCD to be rapidly flushed while clocking the CCD vertically. The relatively high electrical capacity to substrate of the vertical electrodes of the AIMO device places a limitation on the rate that the vertical electrodes may be clocked; however it is the horizontal read-out rate which dominates the overall read-out duration, rather than the vertical clock rate.

The Read-Out Electronics (ROE) unit plus the two CCDs together make up the EIS Camera. Details of the requirements for the EIS Camera is given in document RD1: (MSSL/SLB-EIS/SP05, Design Requirements for the Solar-B EIS Read-Out Electronics).

4 OVERVIEW OF ROE HARDWARE

4.1 Brief description

The EIS camera has two CCDs, named CCD A and CCD B, each with right and left read-out ports. Thus the ROE requires four analogue signal chains in order all four ports to be read out simultaneously. A Correlated Double Sampling (CDS) technique reduces the CCD reset noise to an acceptable level. Each signal chain produces 14-bit parallel data which a Field Programmable Gate Array (FPGA) combines into a 32 Mbps serial stream. This is transmitted to the EIS Instrument Control Unit (ICU) via a high-speed data link in the telescope harness. The ROE has several self-test facilities which are described in detail in the Design Specification for the Clock Sequence Generator (CSG). The CSG is common to both CCDs, for simplicity and elimination of cross-talk. There is a local test CSG in the analogue electronics for pre-flight testing and noise performance evaluation, and a main CSG in the digital electronics which is programmable from the ICU. The main CSG controls the clocks to the CCD and can also generate stim patterns.

4.2 Architecture

The ROE hardware consists of a Motherboard, and three daughter boards: Power PCB, Digital PCB and Analogue PCB. The Motherboard supports a simple pin-to-pin bus structure based around the Hypertac HPF119 (3 row, 119 way) connector. The simple design enables adaptation of the design to other possible projects, with a goal of around 15% spare capacity. The functions of each PCB are listed in section 6.

The block diagram RD2 shows the overall architecture. Communication with ICU is via two types of serial link. A low speed (9.6 kbps) bi-directional asynchronous command and status link, based on the physical specification EIA RS422-A, sends commands to the camera. These commands include master reset, integration time, CCD window origin and size, ports used for read-out, etc. The link receives digitised analogue housekeeping and camera status information.

A high-speed link (32 Mbps) using LVDS technology passes the CCD image data to the ICU. 14-bit data from the four CCD signal chains plus a 2-bit CCD port ID header for each is concatenated into a contiguous 64 bit serial word. An End of Sequence code is appended after each flush or each frame that is read out.

5   DESIGN SPECIFICATIONS

5.1   Specifications *(with references to Requirements Document RD1)*

The ROE design meets the operational requirements listed in RD1. The following references relate to RD1:-

5.1.1   Master Reset (4.1.1) and Power on Reset (4.2.3a).

A Master Reset command from the ICU reboots the ROE, initialises registers to default values, and returns the ROE to its default mode. A power cycle forces the ROE into a Master Reset cycle. Both actions result in the CCD continuously clocking out a new image every 10 s.

5.1.2   Programmability

Provided that the command link is operative, the ICU can take control of the ROE and over-ride the default mode (4.2.3b). Any new register values in the clock sequencer are updated during the CCD integration period (4.2.3d). Commands are listed in RD6: MSSL/SLB-EIS/SP/015, EIS Telecommanding Structure.

5.1.3   Clock speed (4.1.2)

The baseline speed is 32 MHz, to meet requirements of the science data link and CCD clocking rates.

5.1.4   ADC Resolution (4.1.3a)

The baseline ADC is the LTC1419: Resolution 14 bits, DNL < 1 LSB, INL < 1.25 LSB.

5.1.5   Amplifier gain in analogue chain (4.1.3b).

This is set to an overall factor of 12 (including CDS and ADC driver circuitry), given an ADC input dynamic range of 5 V. For 2^{14} (16,384) quantisation steps, this is equivalent to 5.644 e-/LSB, giving a signal of 4.86V at the ADC for a CCD worst case full-well figure of 90k e- (CCD output sensitivity 4.5 µV/e-). The full dynamic range of the ADC corresponds to ~ 92.5 ke-.

5.1.6   CDS specifications (4.1.4a)

The electronic noise of the read-out electronics is set at approximately half the minimum photon shot noise (12 e-) in the long wavelength range, i.e. 6 e-. To achieve this the E2V CCD42-20 spec requires a read-out rate of around 2 µs. A corresponding anti-alias single pole low pass filter with time constant 85 ns is used.

5.1.7   Dump/flush CCD (4.1.5, 4.2.3c)

This is performed by commanding the CCD dump gate (DG) high (+12 V±2 V while clocking the vertical electrodes. In order fully flush the CCD, several (~ 5) successive dump

operations may be required. Single lines, multiple lines, or the entire CCD may be dumped. Some dump operations are inherent in the clock sequences programmed in the Clock Sequence Generator (CSG) on the Digital PCB; others are commanded by separate ICU commands (TBD). The CSG also allows the CCD to start a new integration without a dump beforehand.

5.1.8 Read-out direction (4.1.6)

The CSG defines whether the CCD is read out from the left or right ports of the CCD, or both simultaneously.

5.1.9 CCD horizontal clocking rate (4.1.7a)

In addition to the 2 µs pixel clock rate, the clock sequencer can clock out unwanted (i.e. discard) pixels within a row at a rate of 750 ns per pixel. During pixel discard, the reset gate øR is operated normally to disperse unwanted charge.

5.1.10 Vertical clock phases held high during integration (4.1.7b)

Programmable (TBD): Iø1 only, or Iø1 and Iø2.

5.1.11 CCD bias voltages (4.1.7c)

The CCD bias voltages are separately powered for CCD A and CCD B to prevent fault propagation from one CCD to another. The bias voltages for the left and right output ports of each CCD are common.

Each of the three main bias voltages for each CCD (VOD, VRD and VSS) may be commanded to one of 16 values. Programming codes are issued to the camera from the ICU in standard binary form. (For the PM, an inversion is required within the FPGA on the ROE Analogue PCB, e.g. bias voltage level 7 [0111_2] is issued as 1000_2. For the FM, no inversion is required).

The voltages for both CCDs are monitored by the ROE Power PCB. The actual voltages are given by the following formulae, where n is the step number, form 0 to 15:–

$$VOD = 4.00 \left\lfloor 1 + \frac{330}{58.7 - n} \right\rfloor \text{ V}. \text{ Range 26.5 V to 34.2 V. Approx 0.52 V per step.}$$

$$VRD = 4.00 \left\lfloor 1 + \frac{150}{50.7 - n} \right\rfloor \text{ V}. \text{ Range 15.8 V to 20.8 V. Approx 0.33 V per step.}$$

$$VSS = 4.00 \left\lfloor 1 + \frac{50.9}{47.8 - 1.5n} \right\rfloor \text{ V}. \text{ Range 8.26 V to 12.0 V. Approx 0.25 V per step.}$$

VOG1 has fixed bias at +3V.

VOG2 has 2 programmable levels:–
      Normal responsivity   *VOG2* = +4V, sensitivity 4.5 µV/e–.
      Low responsivity   *VOG2* = +20V, sensitivity 1.5 µV/e–
                    (used for summing well operation)

5.1.12 Window definition (4.2.1a)

Programmable, select window of interest to read out, dump superfluous pixels.

5.1.13 Number of windows (4.2.1b)

A maximum of four, one per read-out port.

5.1.14 Window width and height (4.2.1c)

Programmable to any width within one half of a CCD.

5.1.15 Window height (4.2.1d)

Programmable to a maximum of 512 pixels.

5.1.16 Hardware binning in spatial (V) and spectral (H) directions (4.2.2a)

Vertical binning is achieved by performing multiple row shifts into the read-out register prior to clocking out. Horizontal binning is performed by suppression of the øR clock pulse between pixels, and use of the summing well.

5.1.17 Low responsivity horizontal binning (4.2.2b)

Setting VOG2 to +20V allows up to 540 ke- to be horizontally binned before non-linearity appears in the CCD output amplifier. However the amplifier gain in the analogue chain is fixed at a factor 12, so the maximum charge which can be binned and measured is ~275 ke-.

5.1.18 End of frame marker on science data link (4.2.3g)

This is indicated within the science data by the dead time between each frame of data (implied by a time-out period). The start and end of data associated with each row is indicated by the enable signal becoming inactive.

5.1.19 Overclocking – Horizontal (4.2.4a)

In order to assess CTE in the horizontal direction, the ROE can measure the quantity of charge left behind after the last pixel of each row of a specified window.

5.1.20 Horizontal coordinate register and pixel counter size (4.2.4a)

4096 = 12 bits.

5.1.21 Overclocking – Vertical (4.2.4b)

In order to assess CTE in the vertical direction, the ROE can measure the quantity of charge left behind after the last row of a specified window.

5.1.22 Vertical coordinate register and pixel counter size (4.2.4b)

2048 = 11 bits.

5.1.23 Charge injection (4.2.5)

Not required for FM and not implemented.

5.1.24 Test ports (4.2.6)

Copious analogue signal test points are provided on the Analogue PCB to enable voltages to be set up and monitored during development and testing. Also on the Analogue PCB, test connectors are provided at the FPGA JTAG interface and the digital interface to the motherboard. In addition, a test connector is provided on the Digital PCB.

5.1.25 Stim pattern generator(4.2.7a)

The clock sequencer can generate a stim pattern which is switched to a stimulus source which injects a small signal into the FEE, equivalent to 0.25 and 0.75 of full scale intensity respectively. This is used to check the entire analogue and digital chains. The stim patterns may be applied to the front end of each analogue signal chain, at board test level, unit test level, and pre- and in-flight levels. Complex test image patterns may be uploaded to the ROE via the ICU, or simple 2, 4, or 8 column stripes may be generated at board-level. The stims may be applied whilst clocking out the CCDs.

The stim circuitry is designed to fail safe such that, in the unlikely event of a failure, it is impossible to mask the normal operation of the camera. Separate isolation switches enable/disable the stims, and these are powered from the A and B power rails.

5.1.26 Test image simulator (4.2.7b)

The FPGA on the Analogue PCB can generate a test data pattern which simulates an image. The data is sent directly to the science data links.

5.1.27 Thermal control (4.3.1)

For the CCDs, a combination of a passive radiator and resistive heating under the control of the MHC unit is used. The mechanical design of the CCD mounting should be referred to for more details of the passive radiator. For the ROE unit, a make-up heater powered directly from primary power is incorporated into the ROE box for periods when the ROE is switched off. It is strongly recommended that the unit is left switched on as a means to achieve temperature continuity.

5.1.28 Vertical clock period

A minimum period of 15 µs per row shift is required, which is longer than the estimate stated in version 01 of this document. E2V has confirmed a typical specification of 15µs, with a minimum of 7 µs, for the row shift period. MSSL prefers a minimum of 15 µs. The justification is as follows:

The AIMO version of the CCD42-20 has vertical electrode capacitances which are factor 2.5 times those in the non-pinned versions. Comparing this with the CCD47-20 used in the INTEGRAL OMC camera, a frame transfer style with image area 1024(V) x 1024(H), the capacitances of the vertical electrodes are 5 times greater. Referring to fig. 1, the electrical

model of the CCD42-20 provided by Marconi gives capacitances at each node of a lumped 7-element model as follows:

Iø to substrate capacitance   4.6 nF
Inter-electrode capacitance   1.0 nF

Since all three electrodes are driven from a low impedance source which is decoupled to the substrate, we may estimate a combined capacitance of each electrode to substrate of

C_{tot} = (7 x 4.6 nF) + (2 x 7 x 1 nF) = 46.2 nF.

In order to reduce dissipation within the CCD, an external resistance is added to fix the source impedance. From the E2V CCD42-20 electrode model we see that the lump resistance elements are in the range 22 to 30 Ω for an 8 element model, driven from both ends simultaneously. Thus for the electrode with the maximum resistance (Iø3) the total series resistance feeding the centre is of the order of 150 Ω. At the centre of the lumped model, the capacitance is of the order of 4.6nF + (2 x 1nF) = 6.6 nF. If we add an external resistance of (say) 22 Ω, then to a first approximation the time constant experienced at the centre of the Iø3 electrode will be of the order of 172 x 6.6 x 10^{-9} = 1.2 µs. Thus the width of each vertical clock pulse will need to be at least 10 times this figure, to allow for the settling of the spikes associated with the inter-electrode capacitances.

In order to overcome the problems at the top of the CCD associated with poor CTE due to reduced dynamic full-well, a cycle time of 150 µs was found to provide sufficient margin for the vertical clock triplet. Also to improve the CTE, the vertical clock voltage was increased to 13.5 V. The horizontal clocks were also operated at this voltage.

The dumping of a typical 256 rows will take 256 x 150 µs = 37.5 ms, which is a small overhead compared with the time taken to read out all the pixels. The flushing of the CCD can be performed at a faster rate. It is assumed that multiple (typ. 5) flushes will be performed prior to each exposure. These can be operated at a faster rate.

5.1.29 Commands and telemetry

Camera commands and telemetry are defined in RD: MSSL/SLB-EIS/SP015, EIS Telecommanding Structure.

6 FUNCTIONS OF PCBS

6.1 Analogue PCB

- Video input connectors (2 x MDM 25F)
- RF and clock spike input filtering
- CCD video signal preamplifiers
- CDS electronics: low pass filter, clamp circuitry
- CDS buffers
- ADC drivers / ADC range offset adjustment
- Isolation switches
- ADCs: 14 bit resolution, 1.25 µs max. conversion time
- FPGA functions:
     Parallel to serial data conversion of ADC data
     High speed link generation (32Mbps)
     Programmable control registers and status read-back (address, data, RD,WR)
     Local test CSG including clocks for clamp and isolation switches, ADC convert start, stim signals for front end, and FPGA self-test pattern generation
     Routing of signals from main controller on digital card, including control of CCD bias voltages
     ADC 'nap mode' power switching capability
- Front end stimulus circuitry and stim isolation switches
- CCD bias voltage generation (sub-regulation of +36V)
- Temperature and misc. monitor outputs.
- Misc. test points in video signal chains and digital circuits.

6.2 Digital PCB

- Command and status link
     Connector 9M D-subminiature
     9.6 kbps bi-directional asynchronous
- High speed link (science data)
     Connector 9F D-subminiature
     32 Mbps LVDS
- Power-on reset circuitry
- Command interpreter, status compiler
- CCD clock sequencer electronics for all CCD operations:
     Vertical clocking
     Row dump
     Read-out from 4 CCD ports
     Summing well control
     CDS control, ADC control
- CCD Clock drivers: vertical, row dump, horizontal, summing wells
- Power management, including control of ADC 'nap mode' power switching
- General status and housekeeping functions

6.3 Power PCB

- Power input connector 15M D-subminiature
- Unregulated inputs from converter in ICU
- Low drop-out regulators for secondary power with monitors
- ROE temperature monitors
- 32-channel multiplexor monitor channels
- Refer the table fig. 6 for details of secondary power in and out

7   DETAILED DESIGN

7.1   EMC DESIGN

7.1.1   System compatibility

The design of the camera complies with the spacecraft and instrument EMC requirements in respect of susceptibility and emissions, both conducted and radiated.

7.1.2   Single 32 MHz clock

A single 32 MHz clock is used to derive all signals throughout the camera. This prevents undesirable crosstalk and clock artifacts in the images. Also, the two CCDs are clocked out with identical clocking schemes, although one may be read out of its right port, the other out of its left; this also prevents clock artifacts.

7.1.3   Location and type of Power Converter

The switching power was required to be located away from the camera, in the ICU. The converter is a Buck design, which has significantly lower conducted emissions than a conventional flyback converter for generating multiple outputs. Current and voltage control in the converter produces a very clean output. Located on the Power PCB in the camera is a set of linear sub-regulators to provide very clean supplies for the entire camera unit.

7.1.4   Grounding scheme

The camera grounding complies with the requirements for the EIS instrument grounding as specified in RD3. The internal grounding scheme for the FM camera is shown in fig. 2.

For the PM, the camera grounding scheme was as follows. The demarcation of AGND and DGND on the PM motherboard lay between pins 100, 101, 102 and 103, 104, 105. A separate ground was provided for the CCD clocks (CGND), which was not used in the PM since the CCD clock drivers (located on the Digital PCB) were referenced to AGND.

For the FM, a simpler approach was adopted. CGND is deleted and the demarcation of AGND and DGND lies between pins 55, 56, 57 and 58, 59, 60. This helps prevent cross-coupling of digital current spikes into AGND. DGND and AGND are brought back to a common point on the Power PCB, i.e. the Power PCB ground plane.

A single point ground for connection to the instrument structure ground is provided within the ROE unit. This is made via short wire link between the motherboard and its mounting screw to the ROE box. The location of the link is at the top left-hand corner of the motherboard, close to pin 119 of the HPF119 Hypertac connector which mates to the Analogue PCB. The link may be removed to allow secondary isolation measurements to be made.

The power planes and grounds on individual PCBs are carefully laid out in order to steer noise currents away from sensitive analogue circuitry. At all divisions of areas relating to AGND and DGND it is possible to see 'daylight' through the PCBs.

AGND connects from the read out electronics to the screen of the flexible cables. It was intended to connect the screen to the CCD mount, but this was omitted from the specification for the CCD. The CCD mounts are electrically separated from the support structure, with an easily breakable link to connect the two.

7.1.5   Isolation

To comply with the overall secondary isolation requirements of the instrument, as implied in RD 8 SLB-120 Solar-B Electrical Design Standard, the impedances measured at the ROE with CCDs and harnesses connected shall be within the following limits:

> A capacitance not greater than 2 nF (TBD)
> A resistance less than 50 MΩ (TBD)

These figures are specified so as to meet the overall instrument requirement in the presence of the ICU, MHC and interconnecting harnesses. Thus a design goal for the ROE is a capacitance of one fifth, and a resistance of five times the system level values.

7.1.6   Shielding

The ROE is packaged in a conductive aluminium alloy housing with no significant apertures so as to provide RFI shielding for up to ten times the RF link frequencies (~ 2.3 GHz). All connectors and cables shielded appropriately. The flexible cables to the CCDs should be shielded with a cross hatch mesh spaced at ~ 5 mm, i.e. less than 0.05 of a wavelength of the downlink carrier signal, to take into account harmonics. The shields are connected to AGND on the Analogue PCB and to the CCD mounts which are electrically isolated from the structure.

7.2   Motherboard

Interconnections between the three PCBs of the ROE are via three Hypertac 119-way 3-row female connectors with polarised guides, part no. HPF119NFXEO000. Simple pin-to-pin interconnection is used across all three connectors, making the design simple and adaptable to developing requirements. Fig. 8 shows the pin connections for the FM design.

For the PM, the grounding was originally conceived as follows, and the PM motherboard reflects this. The demarcation of AGND and DGND lies between pins 100, 101, 102 and 103, 104, 105. A separate ground is provided for the CCD clocks (CGND), which is not used in the PM since the CCD clock drivers (located on the Digital PCB) are referenced to AGND. Two groups of ground points are provided to enable the grounds to be connected together and also connected to a structure bond point via a removable coaxial connector through the wall of the box adjacent to the Motherboard.

For the FM, CGND is deleted and the demarcation of AGND and DGND lies between pins 55, 56, 57 and 58, 59,60.

7.3   Analogue PCB

7.3.1   Block diagram

The block diagram fig. 1 shows the architecture of the Analogue PCB. The two CCDs are labeled A and B, with image segments numbered 00, 01, 10, 11, in order of ascending wavelength. There are four analogue chains within the ROE, with ADC data paths which combine such that the right channels of CCDs A and B are multiplexed prior to being converted into serial data and presented to the Digital PCB. The left channels are similarly combined.

7.3.2   Connections to CCDs

The flexible PCB style cables which connect the CCD to the ROE are constructed to minimise crosstalk between sensitive signals from the CCD, to minimise capacitance to AGND, and are shielded from RFI. They are designed to be as short as is practicable so as to minimise degradation of electrode clock signals and video output signals, and to maintain a low impedance bias decoupling points on the Analogue PCB.

The satellite downlink carrier frequency is ~ 2GHz, λ ~ 15cm. Thus to provide adequate shielding a mesh with a spacing of 1.5cm ($\lambda/10$) is required. In reality, harmonics of the carrier will be present, and the 3rd harmonic is likely to be dominant, so a spacing of 0.5cm would be a good choice.

MDM 25-way connectors with flying leads soldered into the Analogue PCB connect to the flexible cables. They are mounted to the ROE housing from the inside. The connectors are specified as having stainless steel shells for robustness and RFI shielding. RF chokes are fitted to the wiring filter unwanted RF energy.

7.3.3   Selection of ADC

The baseline ADC is the LTC1419. Military processed devices are not available from LTC at present, and packaging is plastic SOIC or SSOP. The main reason for selection of this device is that early in the Solar-B programme NASA GSFC commissioned radiation testing of commercial samples and found it to be sufficiently tolerant to gamma and ion flux. MSSL has performed its own radiation and burn-in tests on a commercial batch (without wafer-traceability) procured for flight, and found the devices to pass all the manufacturer's specifications after a total dose of 50 k rad gamma.

The device consumes relatively low power (150mW) and has a fast shut-down and wake-up mode which can be used with power-saving advantage. The baseline package is the SSOP, with 0.025 in lead spacing.

Other faster 14-bit ADCs have been considered, some with on-chip CDS and PGA, such as the 3-channel 7 Msps AD9814 and 15 Msps AD9822 from ADI, manufactured in high volume and low cost (~15 USD) for the high resolution colour scanner and photocopier markets. No radiation performance is known for these devices.

7.3.4   *Choice of CCD clocking scheme*

A number of clocking schemes were considered for use with the LTC1419 ADC. Unfortunately, the relatively long conversion time (1.25µs) of the ADC conflicts with the requirement of a duration of 2µs for the read out of a single pixel (with summing well inactive). Thus there is insufficient time for all necessary events to occur in sequence in the read-out cycle. These are: 1) the reset (øR) of the CCD output node, 2) the clamp switching, and 3) the toggling of the horizontal clock phases (Rø1, Rø2, Rø3) which output the charge associated with the current pixel.

Given the above limitation, a compromise solution was required. The primary design objective in the selection of any clocking scheme was to keep all hazardous switching spikes out of the ADC during the conversion period. Whilst careful grounding of the analogue circuitry is of paramount importance, the main concern was that a small current impulse in the analogue ground (AGND) plane might couple into the ADC and produce an erroneous 14 bit result, especially in the fine (least significant) bits.

Three schemes were considered, all based around a synchronous state machine design with minimum time element T of 125 ns (8MHz). This clock resolution was chosen because of the limitations in the availability of high speed parts suitable for space use, namely the analogue switches for the CDS circuitry and clock drivers for the CCDs. Also 8 MHz it is a convenient sub-multiple of the 32 MHz clock used for the High Speed Link, and independent clocks should be avoided at all cost in any high resolution camera design in order to prevent undesirable artifacts in the images. Thus the minimum overlap of the CCD clocks is 125 ns, exceeding the CCD spec. of 30 ns (min).

Of the three schemes described below, scheme 3 was chosen for the baseline design for EIS. The associated risks were considered at an internal peer review at MSSL. It must be understood that <u>a finite risk exists to the noise performance of the ADC, but that the risk is relatively small.</u>

7.3.4.1   Scheme 1 A simple non-pipelined approach

Exclude the reset, clamp and CCD clocks from the conversion period. This scheme requires 25T (3.125µs), i.e. a reduction in the pixel rate (320 k pix/s).

7.3.4.2   Scheme 2 A pipelined method using a sample-and-hold

Includes a sample-and-hold stage in each analogue chain. This results in a pipelined analog chain of 1 pixel period delay. Pixel n is converted after being sampled and held during the previous pixel time slot. The CCD clocks toggle during the sample period, not during the conversion, and the clamping action of pixel *n+1* straddles the conversion period of pixel *n*, i.e. begins before the conversion the conversion starts, and ends after the conversion is complete. Scheme 2 requires 23T, i.e. 2.875 µs (348 k pix/s).

7.3.4.3   Scheme 3 Overlapping timing scheme using an isolation switch.

The sample-and-hold is replaced by an isolation switch which is effectively a leaky track-and-hold. Its purpose is to isolate the ADC during its busy period from the large transient (up to full-scale) in the video signal resulting from the action of the CCD reset

pulse (øR). The CCD is reset and the clamp action occurs for pixel *n+1* during the conversion of pixel *n*. A timing diagram for the scheme is shown in fig. 3.

This scheme requires 16T to meet the requirement of 2 μs per pixel (500 k pix/s). The following rules were proposed in order to achieve a 2 μs per pixel rate. Of course the ideal mode of operation for any ADC is to have no switching transients in the input signal or associated with the signal ground plane during each conversion period. There are therefore risks associated with scheme 3.

Rule 1

There must be no switching activity <u>during the initial 250 ns</u> acquisition period of the LTC1419 ADC, i.e for 250 ns after the start of the conversion of pixel *n*. However, after the 250 ns point of the each conversion, the following events *are* allowed to occur:

- The isolation switch is activated in order to block the ADC from the ensuing CCD reset transient.
- The CCD reset (øR) for pixel *n+1* occurs.
- The clamp switch is turned on in preparation for pixel *n+1*.

Rule 2

There must be no switching activity <u>after the initial 650ns</u> of the conversion period. From the 650 ns point to the end of the conversion an internal process in the LTC1419 ADC corrects any errors introduced in the conversion of the MSBs. Thus it is potentially hazardous to activate any switches or CCD clocks after the 650 ns point.

Exception to rule 2

The clamp switch is turned off *after* the 650 ns point, during the conversion of the LSBs. This occurs 1T or 2T before the falling edge of Rø3 and øSW. This is deemed safe because there is no charging of the in-series clamp capacitor at this point; the output side of the clamp capacitor floats and thus there is no ground impulse, as compared to when the clamp is turned on, charging the clamp capacitor.

Based on a 2 μs per pixel (500 k pix/s), the scheme requires 16T. The pixel period may need to be extended to 17T or 18T to allow for the clamp and isolation switches to settle. In order to simplify the design and to save power, the isolation switch is implemented by a single analogue switch in the series path between the ADC driver and the ADC input filter capacitor. Given a worst case ADC input leakage current of ±1μA and a filter capacitor of 470 pF the maximum droop will be ~ 2 mV/μs.

7.3.5   *RF and clock spike filter*

The first element in each analogue chain is a low pass filter whose purpose is to attenuate unwanted high frequency noise and switching spikes. This may derive from conducted or radiated susceptibility to RF from the spacecraft communications equipment, and clock spikes from the CCD, either of which might cause the preamplifiers to be driven into a non-linear or saturated condition. An RC element comprising a series resistance of 100 Ω and shunt capacitance of 47 pF attenuates unwanted RF, while the output resistance of the CCD (~600 Ω with the output drain current of the CDD at 2 mA) added to the series 100 Ω produces a pole at 30 ns.

7.3.6   *Video preamplifier and low pass filter*

The baseline video amplifier is the CLC452. This is offered as an alternative to the AD829 proposed in version 01 of this document. The CLC452 is a current feedback device, with nominal 130 MHz bandwidth and 400 V/s slew rate, and capable of driving capacitive loads up to 1 nF, ideal for driving the clamp capacitor in the CDS. Settling time to 0.05% is of the order of 25 ns into a purely resistive 1 kΩ load, and it is hoped that performance to at least 0.1% will be achievable when driving a nominal 100 pF clamp capacitor. While the input noise voltage is not as good as the AD829 (3 nV/Hz compared with 1.5 nV/Hz), its advantages are lower supply current of 3 mA and near rail-to-rail output swing with ±5 V supplies.

The optimum feedback resistance for the CLC452 is 1 kΩ. This is required for optimum performance at frequencies above the 1 MHz region. The EIS PM design uses 4.7 kΩ with a 18 pF shunt and series 1 kΩ. This places a pole at $\tau = 85$ ns (1.9 MHz) and a zero at 18 ns for stability of the current feedback amplifier. However, the FM design uses a simple 1 kΩ feedback resistor with the low pass filter incorporated in the clamp circuitry and subsequent stages.

The clamp switch (HS9-201HSRH) used in the FM design has an on-resistance specified as 50 Ω max. An external 39 Ω resistor adds in series with this and reacts with the 1 nF clamp capacitor to provide a single pole at 79 ns. This acts on the signal only during the clamp phase of each pixel. During the sample phase the low pass filtering is achieved by the ADC input filter.

A single pole filter with time constant τ settles to 1% in 6τ, and to 1 LSB in a 14-bit system in 9.7τ. Thus a settling time of 474 ns is required for pixel-to-pixel modulation of less than 1%, and 766 ns is required for less than 1 LSB. Note that the low pass filter(s) must settle to these levels in both the rsest and the video phases of video pixel. The settling time of the reset and clamp may need to be extended relative to the 2 μs pixel period, at the expense of video level settling time. Also, it may be necessary to reduce the value of τ, at the expense of electronic noise. There is of course a square root relationship, so reducing τ would only slightly increase the noise.

For the FM design, the electronic noise voltage referred to the input of preamplifier stage 1 is calculated below, assuming a 600 Ω source resistance at the CCD, and incorporating the contributions of stages 2 and 3.

CLC452 Input noise voltage	2.85 nV/√Hz
CLC452 Inverting. input current noise	1.66
CLC452 Non-inverting.input current noise	4.95
√(4kTR) noise in inverting. input resistors	1.61
√(4kTR) noise in non-inverting.ip. resistors (incl. CCD source impedance)	3.29
Stage 2 AD744 noise referred to ip (1/6)	2.67
Stage 3 CLC452 noise referred to ip (1/12)	1.50
Total rms noise	7.63 nV/√Hz
Total input noise in a 2.0 MHz bandwidth ($\tau = 79$ ns)	10.78 μV
1 ADC LSB referred to input of stage 1	25.4 μV/LSB
Total input noise in ADC LSBs	0.42 LSB

The above figures neglect the fact that the noise gains at the inverting and non-inverting inputs have a magnitude difference of 1.

7.3.7   Correlated Double Sampler

The CDS circuitry is effectively a clamp and sample arrangement. The clamp operates during the reset phase of each pixel. The clamp is turned on as the CCD reset occurs, and turned off just prior to (one clock cycle T) the start of the video phase (when Rø3 goes low). The sample operation occurs one clock cycle before the end of the video phase (i.e. one clock cycle before the next reset).

An AD744 JFET op amp buffers the clamp capacitor and its very low input bias current results in an extremely low voltage droop on the clamp capacitor. The sample element of the CDS is inherent in the LTC1419 ADC. Note that the isolation switch does not provide a sampling function since it is placed in track mode before the ADC samples the video signal.

Two types of clamp capacitor were tested for the FM, namely ceramic NPO and polystyrene. Whilst the latter type is most commonly employed in sample-hold circuits on account of its low dielectric absorption, no degradation in performance was measurable in the case of the ultra-stable NPO style capacitor. With both types of capacitor, 14 bit resolution could be achieved with a full-scale step applied in the signal. The CDR style NPO chip capacitor is of course a preferred style for flight, being readily available as an established reliability part, and unlike the polystyrene type is resistant to solvents.

The type of analogue switch chosen for the clamp switch in the PM was the DG441. It was hoped that one of theses parts, with MIL-883 processing , would qualify for the FM. The performance of this device, with its low power and low charge injection made it look attractive, and several parts performed well in the PM design. However the devices failed Co_{60} gamma radiation tests even at the 1 k rad level. The rad hard HS9-201HSRH was chosen for the FM. In virtually every performance parameter, except switching speed, this device has poorer performance than the DG441, and consumes significantly higher power (~ 220 mW).

A particular difficulty arose in that the HS9-201HSRH must be powered from a minimum of ±10 V supplies, which presented a phase inversion problem in the AD744 JFET-input buffer amplifier. Thus the AD744 also required its negative rail to be powered from –10 V. This forced the power dissipation of the overall 4-channel design to increase by over 500 mW. The entire analogue chain was originally designed to operate on ±5 V rails. Further, the clamp capacitor had to be increased from 100 pF (in the PM) to 1 nF (in the FM), in order to reduce the voltage steps due to charge injection to an acceptable 20 mV level. The power supply rejection of the HS9-201HSRH was also found to be marginal, but acceptable for the design, on account of the good sub-regulation of the power rails within the Power PCB.

7.3.8   ADC driver

The ADC driver amplifier is a CLC452 operating at gain of –2. This is offset by a reference voltage of +4.06 V applied to its inverting input, to produce a signal at the ADC input in the range –2.5 V to +2.5 V. The +4.06 V reference is available as an output from the ADC in each chain; using this output as the reference guarantees that the offset tracks any drifts in the ADC reference.

An alternative approach would be to feed the $-A_{in}$ of the differential analogue input of the ADC from a +2.5 V reference via a unity gain buffer.

7.3.9   Low pass filter at ADC input

A low pass filter is required at the input to the ADC, to limit the signal bandwidth during the sample phase of the video signal, and to eliminate alias products within the sampled signal. The small signal bandwidth of the ADC sample-and hold circuit is 20 MHz. Any noise or distortion products which are present at the analogue inputs will be summed over the entire bandwidth. The baseline is a simple single-pole RC filter, e.g. 100 Ω plus 470 pF provides a single pole at 3.4 MHz. The 470 pF capacitor also acts as a charge rese

7.4.2   Default mode

The design provides a default mode of operation, which is entered after one of the following conditions: a power-on reset, or a software reset (commanded). The default mode of operation is to set the camera in a continuously running state with an integration time of 10 s (after a flush of the CCD), followed by simultaneous read-out from left and right ports. In normal operation, read-out out is initiated by a command from the ICU.

7.4.3   CCD clock drivers

The vertical and horizontal clock drivers are based on ICL7667 MOSFET driver ICs from Intersil (Harris). These are available as SMD parts (MIL-STD- 883C level B), but without wafer-level radiation testing. Experience of these devices on other programmes such as XMM-OM and INTEGRAL-OMC has proven the broad suitability of these parts. As with these other missions, devices from the flight batch will be tested for radiation tolerance, but only for gamma total dose performance. Foldback current limiters are incorporated in the design to protect the devices against destructive latch-up which could be induced by heavy particles.

To minimise noise coupling directly in the CCDs, all clock drivers are decoupled to AGND. Vertical clock voltages swing from 0V to +13.5V. The horizontal (read-out) clock voltages swing from approximately +0.8V to +13.5V; the slightly positive bias helps prevent leakage of charge from the read-out register back into the bottom row of the storage area. E2V has suggested that this precaution is possibly not necessary with AIMO devices.

The outputs of all clock drivers have damping resistors which perform three functions.
   1) External damping to prevent hazardous undershoots of the clock waveforms, which would allow charge to diffuse in the wrong direction when the previous clock phase is low. Each clock waveform is slightly over-damped to guarantee this.
   2) The damping is adjusted so that the minimum 10% - 90% rise and fall times specified for the CCD are met.
   3) The damping resistors are made as large as is practically possible in order to minimise dissipation within the resistance of the electrodes of the CCD, but not so large that the spikes due to inter-electrode crosstalk are problematical.

Rergarding the Rø and summing well clock waveforms, the capacitance of the summing well electrode is significantly lower than that of the Rø electrodes, and requires a much a larger damping resistance. Undershoots on the Rø clocks would result in poor horizontal CTE; undershoot of the øSW would result in a low responsivity and an apparently high full-well measurement for the CCD, and this was confirmed by experiment.

7.5   Power PCB

This contains sub-regulators for the secondary power supplied from the power converter in the ICU, plus monitor circuitry for the voltages and temperatures in the camera. A 32-channel multiplexer is used to collect the data, and each monitor channel is fed in turn to a single LTC1419 ADC. Only the most significant 8 bits are used. Each sub-regulator is a Low Drop-out (LDO) design, and includes its own current and voltage monitor outputs. Each LVO regulator comprises four op amps; one RH1014 quad op amp is used for each.

The PM design was based upon common power supplies for all four analogue chains on the Analogue PCB. The FM design provides separate power for the pairs of analogue chains for CCD A and CCD B, and for the CCD bias generators and stim circuitry. This will prevent a fault in either CCD or it associated analogue chains from propagating to the other electronics associated with the other CCD.

The circuitry has separate analogue and digital ground planes, which are joined next to the demarcation of the grounds between pins 55, 56, 57 and 58, 59, 60 of the HPF119 Hypertac connector.

Provision is made to power the ROE make-up heater from primary power. The baseline is to route the primary power through the single power connector and wire to an external resistive heater on the connector panel of the unit. Provision is also made to dissipate the heat in an array of parallel 1206 style resistors located around the edge of the board. This is not the preferred method since there is likely to be an EMC issue with the capacitive coupling of primary and secondary grounds in the proximity of the LVO regulators and conducted noise in the primary power feed.

The secondary power inputs to the PCB are fed through common input mode filters to primary ground. These are located on a small land of primary ground close to the power connector. Primary ground does not overlap the secondary power grounds.

8 ELECTRICAL INTERFACES

Pin assignments for the three unit connectors are defined in the table of fig. 7. Connections to the CCD are defined in E2V drawing RD9: DAS 547806 AT, CCD42-20 Interface Drawing (EIS).

9 COMPONENTS AND MATERIALS

The specifications for components and materials are defined in RD10: MSSL/SLB-EIS/SP020.02, Electronic Component Specification.

10 POWER REQUIREMENTS

The table in fig. 6 shows the secondary power requirements for the camera, based on measurements on the PM and adjusted for changes in the design for the FM. Note that for the FM the sub-regulated outputs are separated for CCD A and CC B and their associated signal chains, CCD bias generators and stim circuitry.

Appendix – Tables and figures

Secondary to structure bond point

MOTHERBOARD

AGND plane | **DGND plane**

Note 1. Demarcation between AGND and DGND on motherboard connectors.
For FM, positioned between pins 55, 56, 57 and 58, 59, 60.
(PM position was between pins 94, 95, 96 and 97, 98, 99.)

Note 2. At each CCD there is galvanic isolation between invar mounts and substrate, and approx 1nF capacitance.
Provision is made on the analogue card to bond AGND to the ROE box, as alternative to the bond point if required.

POWER PCB
(Note 1)

Analogue regulators   Digital regs.

Single GND plane, separate anlg. & dig. areas

| +5VA +5VB | −5VA −5VB | | +5VD |
| +12VD2 +12VD3 | +12VA +12VB | | +2.5VD |

+36VA +36VB   **Linear regulators and filters**

Approx routes of power feed tracks

Power conn.   Make-up heater

Sec rtns B,C,D   Pri rtn.

DIGITAL PCB
(Note 1)

AGND plane   **DGND plane**

+12VD2 +12VD3   +5VD

CCD clock drivers

Command decoder, CCD clock sequence gen, 32Mbps LVDS link drivers

Command & status conn.   Science data conn.

CCD A (Note 2)
CCD B (Note 2)

ANALOGUE PCB
(Note 1)

AGND plane   **DGND plane**

+5VA +5VB   −5VA −5VB   +5VD
+12VA +12VB   +36VA +36VB   +2.5VD

Analogue signal chains

FPGA: Test clock gen, 32Mbps data link

Solar B EIS Camera Grounding Scheme - FM
Phil Thomas MSSL-UCL July 2002

Fig. 1 Camera Grounding Configuration
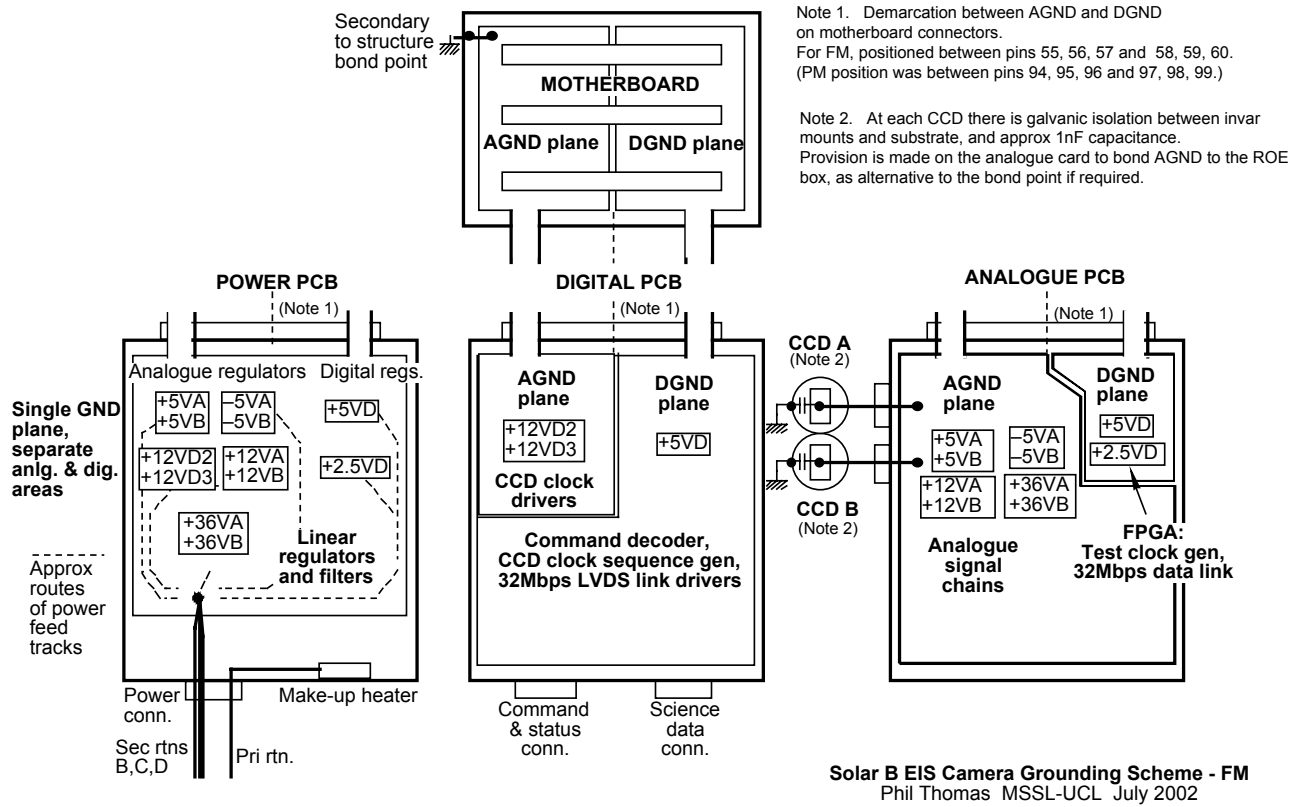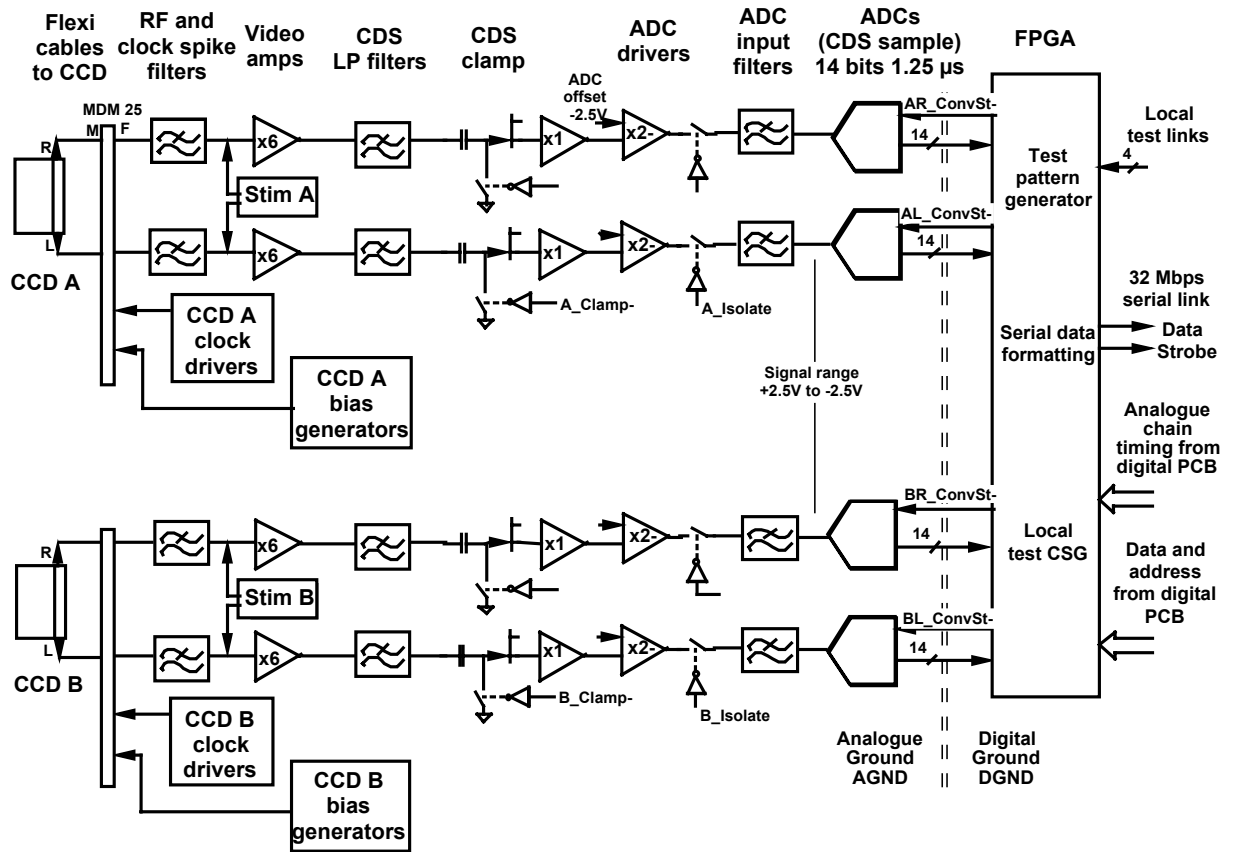MSSL/SLB-EIS/DD/021.01EIS

Fig. 2   Analogue PCB Block Diagram
MSSL/SLB-EIS/DD/022.01EIS
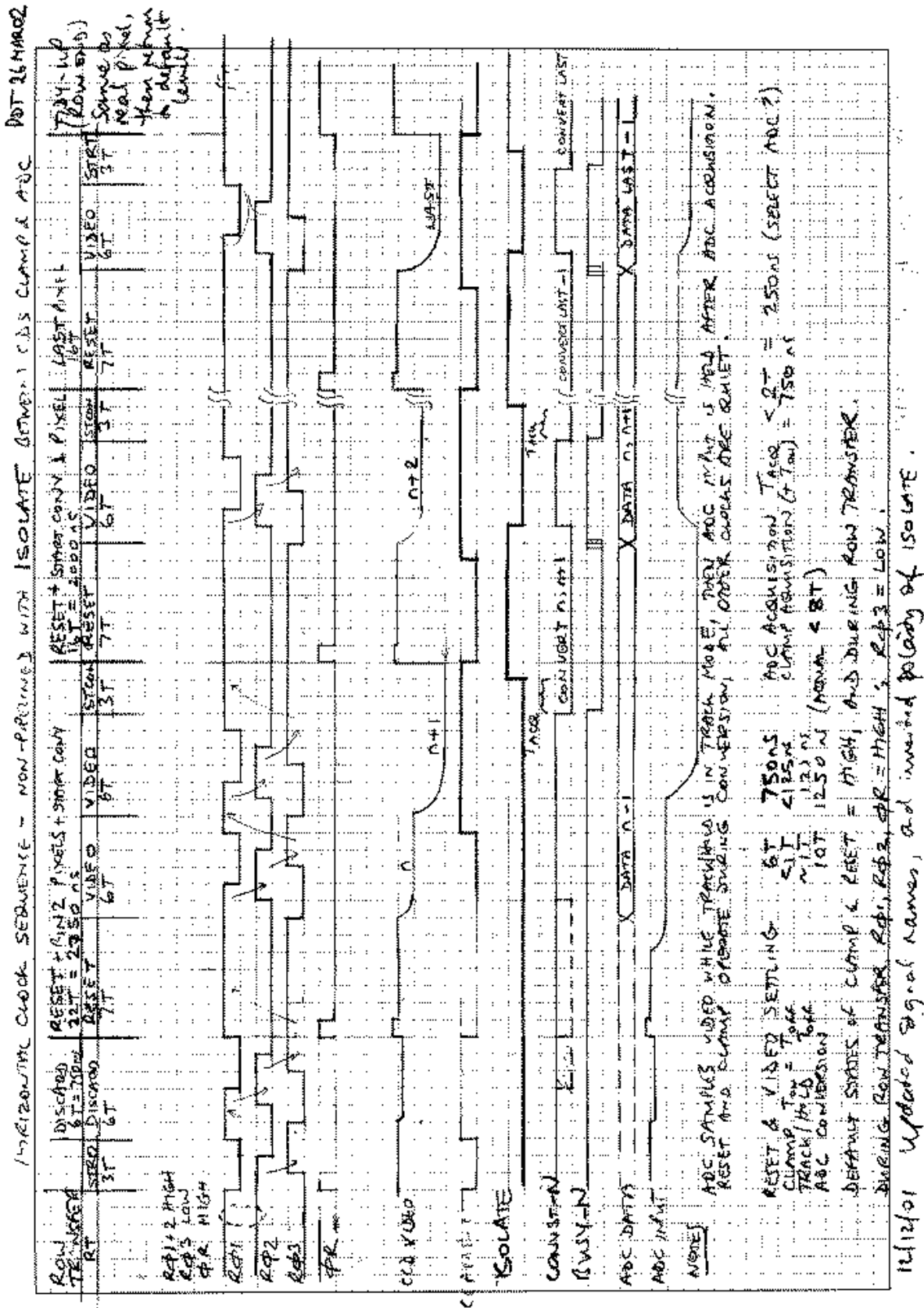
Fig. 3   Timing diagram for overlapping clocking scheme with isolation switch
(programmable control registers in FPGA on Digital PCB)
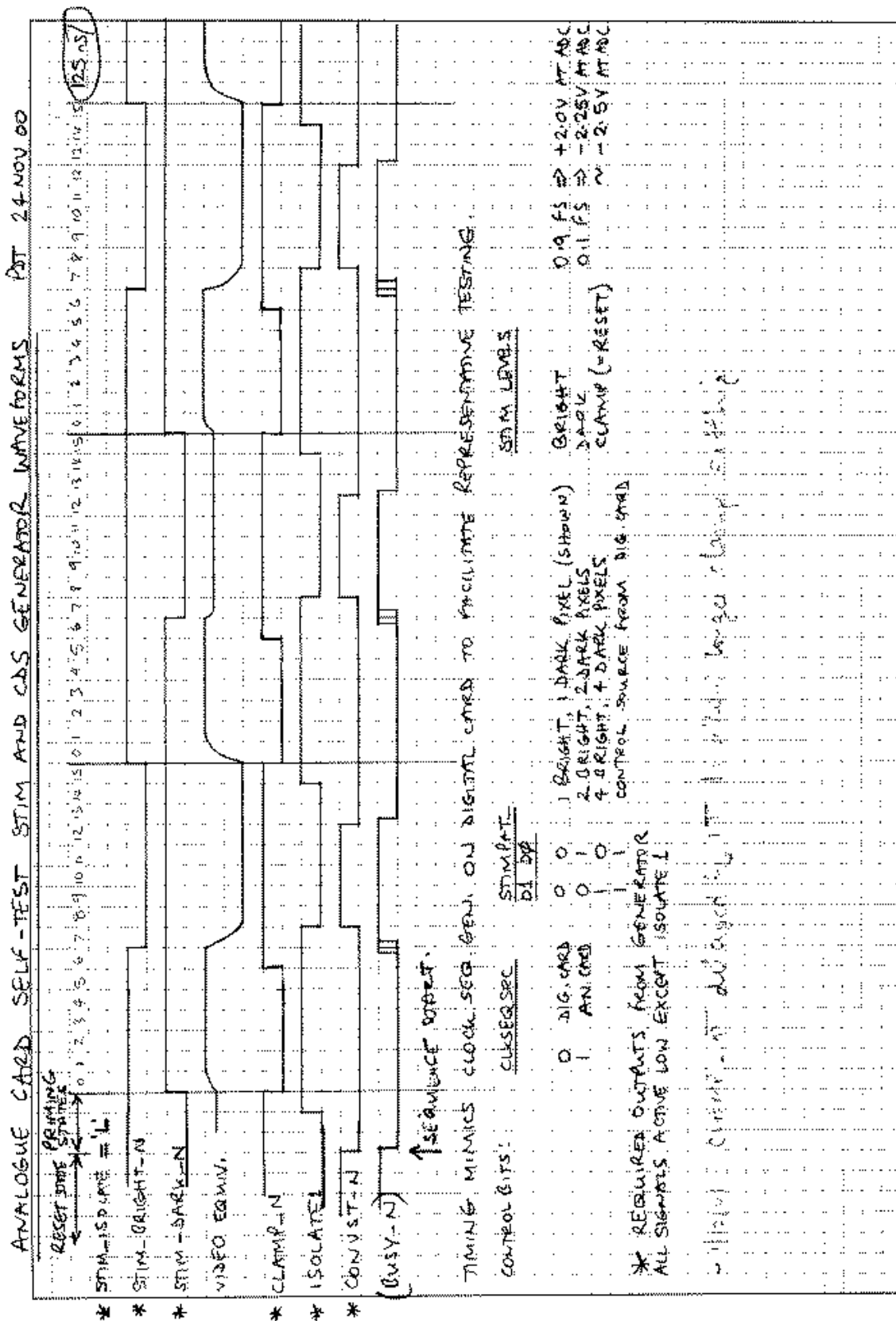
Fig. 4 Timing diagram for local test clock sequence generator
(programmed in FPGA on Analogue PCB)

Fig. 5   Block diagram of local FPGA
(on Analogue PCB)
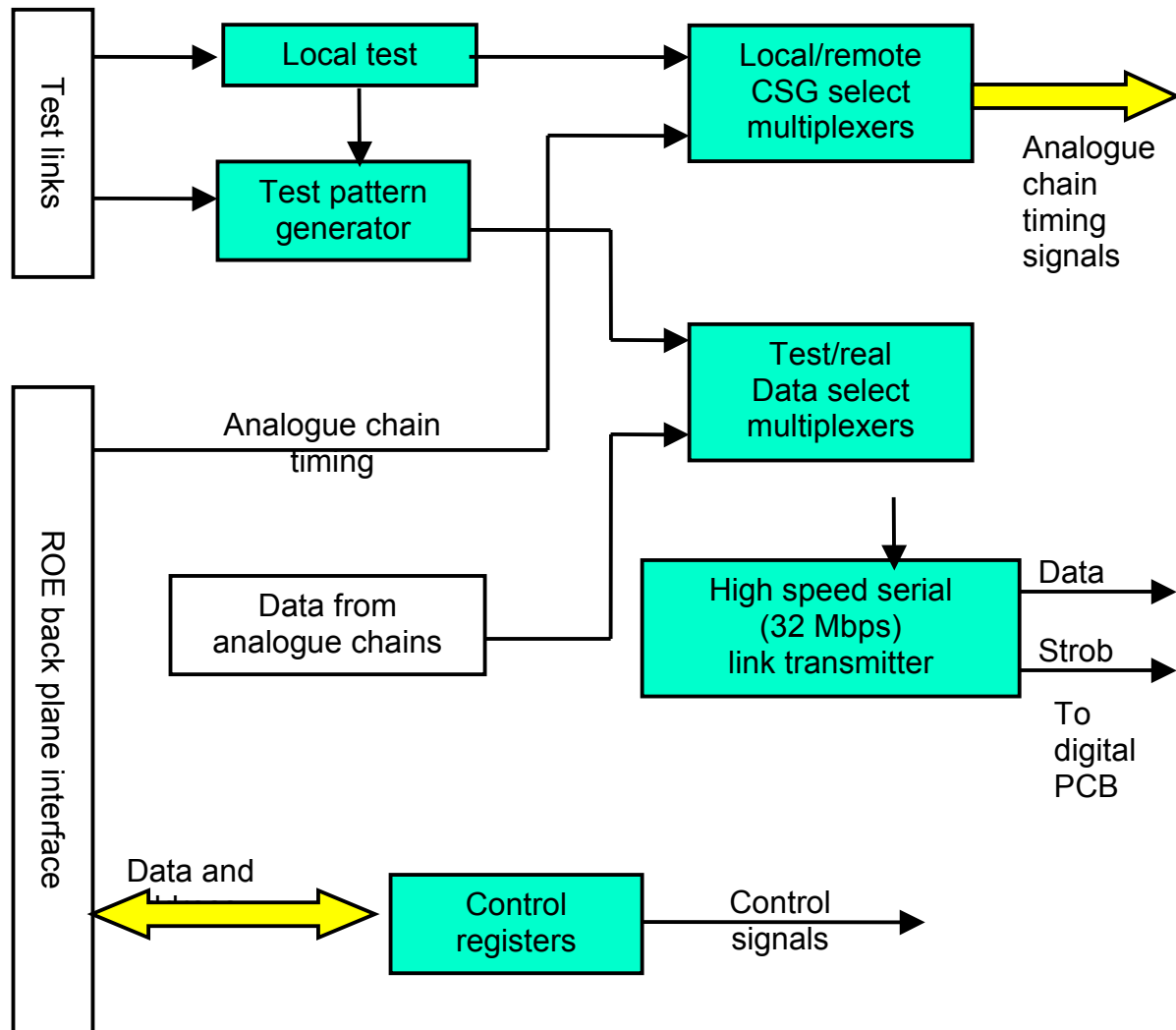
Output voltage	Incoming voltage	Line Identity	Ground identity	Return line	Minimum current	Average current	Peak current	Exp' EOM current
(+)5V0	(+)7V0	(+)5VD	B	DGND	30mA	100mA	100mA	120mA
(+)2V5	(+)7V0	(+)2.5VD	B	DGND	10mA	60mA	60mA	72mA
(+)5V0	(+)8V0	(+)5VA	C	AGND	45mA	50mA	60mA	60mA
(+)5V0	(+)8V0	(+)5VB	C	AGND	45mA	50mA	60mA	60mA
(-)5V0	(-)8V0	(-)5VA	C	AGND	65mA	70mA	70mA	84mA
(-)5V0	(-)8V0	(-)5VB	C	AGND	65mA	70mA	70mA	84mA
(+)36V0	(+)39V0	(+)36VA	C	AGND	5mA	8mA	10mA	12mA
(+)36V0	(+)39V0	(+)36VB	C	AGND	5mA	8mA	10mA	12mA
(+)12V0	(+)13V5	(+)12VA	D	AGND	10mA	15mA	15mA	18mA
(+)12V0	(+)13V5	(+)12VB	D	AGND	10mA	15mA	15mA	18mA
(+)12V0	(+)12VA	(+)12VD2	D	AGND	20mA	65mA	90mA	78mA
(+)12V0	(+)12VB	(+)12VD3	D	AGND	20mA	65mA	90mA	78mA

Fig. 6 Voltage and current requirements for FM camera
(inputs and outputs of Power PCB)

Digital PCB

Function	*Pin*
Command & Telemetry	**EIS-ROE4 9M D-sub**
Cmd+	7
Cmd-	3
HK+	2
HK-	1
Gnd	9
Chassis	5
Note: Cmd & HK swapped wrt the MHC	

Science Data	**EIS-ROE3 9F D-sub**
Sdata+	4
Sdata-	9
Strobe+	2
Strobe-	6
Gnd strobe	1
Gnd	3
Gnd Sdata	5
Chassis	7

Power PCB

Function	*Pin*
Power	**EIS-ROE5 15M D-sub**
+8V	2
-8V	3
+39V	4
-13V	6
+7V	7
Chassis	1
Chassis	8
Gnd B	15
Gnd C	9
Gnd C	10
Gnd C	11
Gnd D	13

Note: Connector polarity refers to the unit, not the cable

Fig. 7 Pin assignments of connectors on ROE unit

Power PCB SK1		Digital PCB SXK2		Analogue PCB SK3	
Pin no.	Signal name	Pin no.	Signal name	Pin no.	Signal name
Inner row		Inner row		Inner row	
1	DGND	1	DGND	1	DGND
4	+5VD	4	+5VD	4	+5VD
7	SYS_RESET_N	7	SYS_RESET_N	7	SYS_RESET_N
10	SYS_CLK	10	SYS_CLK	10	SYS_CLK
13	DGND	13	DGND	13	DGND
16	SHUT_DOWN	16	SHUT_DOWN	16	SHUT_DOWN
19	+2.5VD	19	+2.5VD	19	+2.5VD
22	-10VA_MON	22	-10VA_MON	22	-10VA_MON
25	-10VB_MON	25	-10VB_MON	25	-10VB_MON
28	MON3	28	MON3	28	MON3
31	MON4	31	MON4	31	MON4
34	+13.5VRET	34	+13.5VRET	34	+13.5VRET
37	AN_TEMP_MON	37	AN_TEMP_MON	37	AN_TEMP_MON
40	A_VOD_MON	40	A_VOD_MON	40	A_VOD_MON
43	A_VRD_MON	43	A_VRD_MON	43	A_VRD_MON
46	A_VSS_MON	46	A_VSS_MON	46	A_VSS_MON
49	B_VOD_MON	49	B_VOD_MON	49	B_VOD_MON
52	B_VRD_MON	52	B_VRD_MON	52	B_VRD_MON
55	B_VSS_MON	55	B_VSS_MON	55	B_VSS_MON
58	+12VD2	58	+12VD2	58	+12VD2
61	+12VD3	61	+12VD3	61	+12VD3
64	SPARE_ANLG_POWR	64	SPARE_ANLG_POWR	64	SPARE_ANLG_POWR
67	SPARE_ANLG_SIG1	67	SPARE_ANLG_SIG1	67	SPARE_ANLG_SIG1
70	SPARE_ANLG_SIG2	70	SPARE_ANLG_SIG2	70	SPARE_ANLG_SIG2
73	SPARE_ANLG_SIG3	73	SPARE_ANLG_SIG3	73	SPARE_ANLG_SIG3
76	HK_MUX_SEL6	76	HK_MUX_SEL6	76	HK_MUX_SEL6
79	HK_DATA_RDY	79	HK_DATA_RDY	79	HK_DATA_RDY
82	HK_CONVST_N	82	HK_CONVST_N	82	HK_CONVST_N
85	HK_MUX_SEL0	85	HK_MUX_SEL0	85	HK_MUX_SEL0
88	HK_MUX_SEL1	88	HK_MUX_SEL1	88	HK_MUX_SEL1
91	HK_MUX_SEL2	91	HK_MUX_SEL2	91	HK_MUX_SEL2
94	HK_MUX_SEL3	94	HK_MUX_SEL3	94	HK_MUX_SEL3
97	HK_MUX_SEL4	97	HK_MUX_SEL4	97	HK_MUX_SEL4
100	HK_MUX_SEL5	100	HK_MUX_SEL5	100	HK_MUX_SEL5
103	+5VA	103	+5VA	103	+5VA
106	-5VA	106	-5VA	106	-5VA
109	+12VA	109	+12VA	109	+12VA
112	-10VA	112	-10VA	112	-10VA
115	+36VA	115	+36VA	115	+36VA
118	AGND	118	AGND	118	AGND
Middle row		Middle row		Middle row	
2	DGND	2	DGND	2	DGND
5	+5VD	5	+5VD	5	+5VD
8	LINK_DATA	8	LINK_DATA	8	LINK_DATA
11	+13.5V1	11	+13.5V1	11	+13.5V1
14	DGND	14	DGND	14	DGND
17	RD_EN	17	RD_EN	17	RD_EN
20	+2.5VD	20	+2.5VD	20	+2.5VD
23	D0	23	D0	23	D0
26	D2	26	D2	26	D2
29	D4	29	D4	29	D4
32	D6	32	D6	32	D6
35	+13.5VRET	35	+13.5VRET	35	+13.5VRET
38	A0	38	A0	38	A0
41	A2	41	A2	41	A2
44	A4	44	A4	44	A4
47	CLAMP_N	47	CLAMP_N	47	CLAMP_N
50	CONVST_N	50	CONVST_N	50	CONVST_N
53	STIM_BRIGHT_N	53	STIM_BRIGHT_N	53	STIM_BRIGHT_N
56	EOS	56	EOS	56	EOS
59	+12VD2	59	+12VD2	59	+12VD2
62	+12VD3	62	+12VD3	62	+12VD3
65	SPARE_ANLG_PWR	65	SPARE_ANLG_PWR	65	SPARE_ANLG_PWR
68	B_DG	68	B_DG	68	B_DG
71	B_Iø2	71	B_Iø2	71	B_Iø2
74	B_Rø2_R	74	B_Rø2_R	74	B_Rø2_R
77	B_Rø3	77	B_Rø3	77	B_Rø3
80	B_Rø2_L	80	B_Rø2_L	80	B_Rø2_L
83	B_øSW_L	83	B_øSW_L	83	B_øSW_L
86	A_DG	86	A_DG	86	A_DG
89	A_Iø2	89	A_Iø2	89	A_Iø2
92	A_Rø2_R	92	A_Rø2_R	92	A_Rø2_R
95	A_Rø3	95	A_Rø3	95	A_Rø3
98	A_Rø2_L	98	A_Rø2_L	98	A_Rø2_L
101	A_øSW_L	101	A_øSW_L	101	A_øSW_L
104	+5VA	104	+5VA	104	+5VA
107	-5VA	107	-5VA	107	-5VA
110	+12VA	110	+12VA	110	+12VA
113	-10VA	113	-10VA	113	-10VA
116	+36VA	116	+36VA	116	+36VA
Outer row		Outer row		Outer row	
3	DGND	3	DGND	3	DGND
6	+5VD	6	+5VD	6	+5VD
9	LINK_STROBE	9	LINK_STROBE	9	LINK_STROBE
12	+13.5V2	12	+13.5V2	12	+13.5V2
15	DGND	15	DGND	15	DGND
18	WR_EN	18	WR_EN	18	WR_EN
21	+2.5VD	21	+2.5VD	21	+2.5VD
24	D1	24	D1	24	D1
27	D3	27	D3	27	D3
30	D5	30	D5	30	D5
33	D7	33	D7	33	D7
36	+13.5VRET	36	+13.5VRET	36	+13.5VRET
39	A1	39	A1	39	A1
42	A3	42	A3	42	A3
45	A5	45	A5	45	A5
48	ISOLATE	48	ISOLATE	48	ISOLATE
51	HK_SHTDWN_N	51	HK_SHTDWN_N	51	HK_SHTDWN_N
54	HK_OE_N	54	HK_OE_N	54	HK_OE_N
57	STIM_DARK_N	57	STIM_DARK_N	57	STIM_DARK_N
60	+12VD2	60	+12VD2	60	+12VD2
63	+12VD3	63	+12VD3	63	+12VD3
66	SPARE_ANLG_PWR		SPARE_ANLG_PWR		SPARE_ANLG_PWR
69	B_øSW_R	69	B_øSW_R	69	B_øSW_R
72	B_Iø3	72	B_Iø3	72	B_Iø3
75	B_Iø1	75	B_Iø1	75	B_Iø1
78	B_Rø1_R	78	B_Rø1_R	78	B_Rø1_R
81	B_Rø1_L	81	B_Rø1_L	81	B_Rø1_L
84	B_øR	84	B_øR	84	B_øR
87	A_øSW_R	87	A_øSW_R	87	A_øSW_R
90	A_Iø3	90	A_Iø3	90	A_Iø3
93	A_Iø1	93	A_Iø1	93	A_Iø1
96	A_Rø1_R	96	A_Rø1_R	96	A_Rø1_R
99	A_Rø1_L	99	A_Rø1_L	99	A_Rø1_L
102	A_øR	102	A_øR	102	A_øR
105	+5VB	105	+5VB	105	+5VB
108	-5VB	108	-5VB	108	-5VB
111	+12VB	111	+12VB	111	+12VB
114	-10VB	114	-10VB	114	-10VB
117	+36VB	117	+36VB	117	+36VB
119	AGND	119	AGND	119	AGND

Fig. 8 ROE Motherboard pin assignments