Solar B - EIS

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SOLAR B – EIS Read Out Electronics: Electrical Design Specification

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Contents

1 INTRODUCTION

The camera in the EUV imaging spectrometer (EIS) on the Solar-B spacecraft contains two CCDs, covering wavelengths TBD and TBD. The CCDs, type CCD42-20, are procured from Marconi Applied Technology (ex-EEV). The devices are back-thinned, operate in full-frame mode, size 1024(Y) x 2048(X) pixels, with readout out ports at both ends of the read out register; pixel resolution is 13.5 x 13.5 μm. The CCDs are fabricated for Advanced Inverted Mode Operation (AIMO), i.e. MultiPhase Pinned (MPP). This allows the devices to be operated at a moderately low temperature (-55C) while minimising dark current.

Under the control of the EIS Instrument Control Unit (ICU), the Read Out Electronics (ROE) extracts images from the two CCDs and presents image data in serial form to the ICU.

EIS will obtain plasma velocities to an accuracy of <= 10 km s^{-1} along with temperatures and densities in the transition region and corona at <2 arc sec resolution. EIS consists of a multi-layer coated single mirror telescope, and a stigmatic imaging spectrometer incorporating a multilayer coated diffraction grating. The image produced by the primary mirror is imaged onto an entrance slit/slot and the light which passes through this spectrometer aperture is dispersed and re-imaged in the focal plane of two CCDs.

Details of the requirements for the EIS Camera unit is given in document RD1 (MSSL/SLB-EIS/SP05, Design Requirements for the Solar-B EIS Read Out Electronics).

2 REFERENCE DOCUMENTS

RD1 MSSL/SLB-EIS/SP05 Design Requirements for the Solar-B EIS Read Out Electronics
RD2 MSSL/SLB-EIS/DD/004.01 CCD Camera Block Diagram
RD3 MSSL/SLB-EIS/DD/002.01 Grounding Configuration
RD4 MSSL/SLB-EIS/xxxx Camera Commands and Telemetry

3 ABBREVIATIONS

ADC	Analogue to Digital Converter
AGND	Analogue (Signal) Ground
AIMO	Advanced Inverted Mode Operation
CCD	Charge Coupled Device
CDS	Correlated Double Sampler
CGND	CCD Clock Ground
ComGND	Common Ground
CTE	Charge Transfer Efficiency
DG	CCD Dump Gate
DGND	Digital Ground
EIS	Extreme UV Imaging Spectrometer
FEE	Front End Electronics

FPA	Focal Plane Assembly
FPGA	Field Programmable Gate Array
ICU	Instrument Control Unit
Iø	Image (Vertical) Clock Phase
LVDS	Low Voltage Differential Signaling
MDM	Micro-D connector (with metal shell)
MHC	Mechanisms and Heaters Controller
MPP	Multi-Phase Pinned
øR	Reset Clock Pulse
OS	CCD Output Source
PISO	Parallel In Serial Out register
Rø	Read Out Register (Horizontal) Clock Phase
ROE	Read Out Electronics
SW	CCD Summing Well
TBC	To Be Confirmed
TBD	To Be Defined
VOD	CCD bias Voltage at Output Drain
VOG	CCD bias Voltage at Output Gate
VRD	CCD bias Voltage at Reset Drain
VSS	CCD bias Voltage at Substrate

4 OVERVIEW OF ROE HARDWARE

4.1 Structure

The block diagram RD2 shows the overall architecture. Communication with the Instrument Control Unit (ICU) is via two types of serial link. A low speed (9.6 kbps) bi-directional asynchronous command and status link based on the EIA RS422-A (TBD) physical specification sends commands to the camera, e.g. master reset, integration time, CCD window origin and size, ports used for read out, etc., and receives digitised analogue housekeeping and camera status information. A dual high speed (16 Mbps) science link based on LVDS technology passes the CCD image data to the ICU.

The ROE consists of a Mothercard, and three daughter boards: Power Card, Digital Card and Analogue Card. The Mothercard supports a simple pin-to-pin bus structure based around the Hypertac HPF120 (3 row, 120 way) connector. The simple design enables adaptation of the design to other possible projects, with a goal of around 15% spare capacity. The functions of each card are listed in section 6.

5 DESIGN SPECIFICATIONS

5.1 Specifications with reference to Requirements Document RD1

The ROE design meets the operational requirements listed in RD1. The following references relate to RD1:-

5.1.1 Master Reset (4.1.1) and Power on Reset (4.2.3a).

A Master Reset command from the ICU reboots the ROE, initialising registers to default values and returns the ROE to the default mode. A power cycle forces the ROE into a Master Reset cycle. Both actions result in the CCD continuously clocking out a new image every 10 s.

5.1.2 Programmability

Provided that the command link is operative, the ICU can take control of the ROE and over-ride the default mode (4.2.3b). Any new register values in the clock sequencer are updated during the CCD integration period (4.2.3d).

5.1.3 Clock speed (4.1.2)

The baseline is 16MHz, to meet the requirement of the science data link and CCD clocking requirements. Possibly 32 MHz divided by 2.

5.1.4 ADC Resolution (4.1.3a)

14 bits. The baseline ADC is the LTC1419 (TBC).

5.1.5 Amplifier gain in analogue chain (4.1.3b).

This is set to an overall factor of 12 (including CDS and ADC driver circuitry), given an ADC input dynamic range of 5 V. For 16,384 quantisation steps (14 bits), this is equivalent to 5.644 e-/DN, giving a signal of 4.86V at the ADC for a CCD full well of 90k e- (CCD output sensitivity 4.5 μV/e-). The full dynamic range of the ADC corresponds to ~92.5 ke-.

5.1.6 CDS specifications (4.1.4a)

Read out electronic noise is set at approx half the minimum photon shot noise (12 e-) in the long wavelength range, i.e. 6 e-. To achieve this the Marconi CCD spec requires a read out rate of around 2 μs. A corresponding anti-alias single pole (TBC) low pass filter with time constant 100 ns (TBC) is provided.

5.1.7 Dump/flush CCD (4.1.5, 4.2.3c)

This is performed by commanding the CCD dump gate (DG) high (+12 V±2 V) for at least 10μs while holding the vertical clock phases in the appropriate states. In order fully flush the CCD, several (~5) successive dump operations are required. Single lines, multiple lines, or the entire CCD may be dumped. Some dump operations are inherent in the clock sequences programmed in the clock sequencer (on the Digital Card). Others are commanded by separate ICU commands. The clock sequencer also allows the CCD to start a new integration without a dump beforehand.

5.1.8 Read out direction (4.1.6)

The clock sequencer defines whether the CCD is read out from the left or right ports of the CCD, or both simultaneously.

5.1.9 CCD horizontal clocking rate (4.1.7a)

In addition to the 2 μs pixel clock rate, the clock sequencer can clock out unwanted pixels within a row at a 1 μs rate. In this case, the reset gate øR is operated normally to disperse unwanted charge.

5.1.10 Vertical clock phases held high during integration(4.1.7b)

Programmable (TBC): Iø1 only, or Iø1 and Iø2.

5.1.11 CCD bias voltages (4.1.7c)

Programmable bias(separate for CCD A and CCD B):
VOD +26.5 to +34 V, 16 steps, 0.5V per step.
VRD +17.25 to +21 V, 16 steps, 0.25 V per step.
VSS +8.25 to +12 V, 16 steps, 0.25 V per step.
VOG2 2 levels, +4V (high responsivity, 4.5 μV/e-), or +20V (low responsivity, 1.5 μV/e-).
Fixed bias:
VOG1 +3V.

5.1.12 Window definition (4.2.1a)

Programmable, select window of interest to read out, dump superfluous pixels.

5.1.13 Number of windows (4.2.1b)

A maximum of four, one per read out port.

5.1.14 Window width and height (4.2.1c)

Programmable to any width within one half of a CCD.
(TBC: “both windows on the CCD may be the same height”)

5.1.15 Window height (4.2.1d)

Programmable to a maximum of 512 pixels.

5.1.16 Hardware binning in spatial (V) and spectral (H)directions (4.2.2a)

Vertical binning is achieved by performing multiple row shifts into the read out register prior to clocking out. Horizontal binning is performed by suppression of the øR clock pulse between pixels.

5.1.17 Low responsivity horizontal binning (4.2.2b)

Setting VOG2 to +20V allows up to 540 ke- to be horizontally binned before non-linearity appears in the CCD output amplifier. However the amplifier gain in the analogue chain is fixed at a factor 12,so the maximum charge which can be binned and measured is ~275 ke-.

5.1.18 End of frame marker on science data link (4.2.3g)

This is indicated within the science data by the dead time between each frame of data (i.e. implied by a time-out period). The start and end of data associated with each row is indicated by the enable signal becoming inactive.

5.1.19 Overclocking – Horizontal (4.2.4a)

In order to assess CTE in the horizontal direction, the ROE can measure the quantity of charge left behind after the last pixel of each row of a specified window.

5.1.20 Horizontal coordinate register and pixel counter size (4.2.4a)

4096 = 12 bits.

5.1.21 Overclocking – Vertical (4.2.4b)

In order to assess CTE in the vertical direction, the ROE can measure the quantity of charge left behind after the last row of a specified window.

5.1.22 Vertical coordinate register and pixel counter size (4.2.4b)

2048 = 11 bits.

5.1.23 Charge injection (4.2.5)

(TBC) Charge may be injected into the CCD read out register by applying a voltage pulse to the reset drain RD (a few volts less than VRD) clocking the output register CCD backwards. See application note from Tim Eaton of Marconi, email dated dd/mm/00.

5.1.24 Test ports (4.2.6)

Four analogue signal test ports are provided on the outside of the ROE, via coaxing connectors on the Analogue Card. The signals are the amplified CCD signals, after low pass filtering, just prior to the CDS circuitry. Multiple test points are fitted to the Analogue Card to enable voltages to be set up and monitored during development and testing. In addition, a test connector is provided on the Digital Card.

5.1.25 FEE stim pattern generator(4.2.7a)

The clock sequencer can generate a stim pattern (digital 0 or 1) which is switched to a stimulus source which injects a small signal into the FEE, equivalent to 0.25 and 0.75 of full scale intensity respectively. This is used to check the entire analogue and digital chains.

5.1.26 Test image simulator (4.2.7b)

The Digital Card can generate a data set which simulates an image. The data is sent directly to the science data links.

5.1.27 Thermal control (4.3.1)

TBD

5.2 Other specifications

5.2.1 Vertical clock period – 12 µs minimum.

The AIMO version of the CCD42-20 has vertical electrode capacitances which are factor ~2.5 times those in the non-pinned version. Compare this with the CCD47-20 used in the INTEGRAL OMC camera (frame transfer style, image area 1024(V) x 1024(H)), the capacitances of the vertical electrodes are 5 times greater. The electrical model of the CCD42-20 provided by Marconi gives capacitances at each node of a 7 lumped element model as follows:

Iø to substrate 4.6 nF
Interelectrode 1 nF

Since all three electrodes are driven from a low impedance source which is decoupled to the substrate, we may estimate a combined capacitance of each electrode to substrate of

Ctot = (7 x 4.6 nF) + (2 x 7 x 1 nF) = 46.2 nF.

Now in order to minimise dissipation within the CCD, an external resistance is employed to fix the source impedance. From the CCD electrode model we see that the lump resistance

elements are in the range 22 to 30 • for an 8 element model, driven from both ends simultaneously. Total series resistance is of the order of 120 • in the worst case, being Iø3. At the centre of the lumped model, the capacitance is of the order of 4.6nF + (2 x 1nF) = 6.6 nF. Therefore to a first approximation , the time constant seen at the centre of the Iø3 electrode will be of the order of 120 x 6.6 x 10^{-9} = 792 ns. The actual figure will be closer to 1 µs due to the effect of the other elements. If we allow 6 time constants for settling, then the minimum vertical clock period will be 2 x 6 x 1 µs = 12 µs. A full vertical dump will take 1024 x 12 µs = ~12 ms. The overhead in reading out a full image 512(V) x 1024(H) will be ~6 ms in a total read out time of ~550 ms, i.e. ~2%.

5.3 Commands and telemetry

Camera commands and telemetry are defined in RD4.

6 FUNCTIONS OF PCBS

6.1 Power Card

Power input connector (15F D TBD).
Unregulated Inputs (TBD) from converter in ICU – approx voltages: +7V, +15V, -8V.
Low drop-out regulators for secondary power:-
Regulated outputs (TBD): +5VD, +5VADC, -5VADC, +12VA, -7VA
Boost converter output: +36V for CCD VOD and VRD bias voltages.
Analogue voltage and current monitors for camera electronics.
CCD temperature monitors (TBD)

6.2 Digital Card

Command and status link (TBD connector) – low speed 9.6 kbps bi-directional asynchronous.
Command registers and boot circuitry.
Science data links (TBD connector) – dual high speed 16 Mbps
CCD clock sequencer electronics for all CCD operations: vertical shift, row dump, readout from 4 CCD ports, readout register charge injection, summing well control.
Test pattern generation: stimulus for front end electronics (FEE), science data link test pattern.
Correlated Double Sampler (CDS) control, Analogue to Digital Converter (ADC) control, Parallel to Serial (PISO) and data bus control.
CCD bias voltage control: VOD, VRD, VSS, VOG2.
Power management, including control of ADC ‘nap mode’ power switching.
General status and housekeeping functions.
Test connector.

6.3 Analogue Card

Video input connectors (25F MDM x2)
Video signal input filtering
CCD video signal preamplifiers
CDS electronics: low pass filter, clamp circuitry.
Clamp buffer/ADC driver circuitry.
Sample circuitry and digitisation to 14 bits (ADCs).
PISOs and serial data switching.

CCD Clock drivers: vertical, row dump, horizontal, summing wells.
Charge injection (TBC) and FEE stimulus circuitry.
CCD bias voltage generation.
ADC 'nap mode' power switching.
CCD temperature monitor inputs (TBD).
Test connectors- video signals at CDS inputs.

7 DETAILED DESIGN

7.1 Mothercard

Interconnections between the three PCBs of the ROE are via three Hypertac 3-row female connectors with polarised guides, part no. HPF119NFXEO000. Simple pin-to-pin interconnection is used across all three connectors, making the design simple and adaptable to developing requirements. At least one group of ground points is provided to enable the various grounds to be connected together and also connected to a structure bond point via a removable coaxial connector through the wall of the box adjacent to the Mothercard.

7.2 Digital Card

(TBD) The baseline design incorpoates a number of FPGAs and RAM ICs to perform the functions listed in section 4.2.2.

A counter-timer is provided for the default mode, i.e. continuously running with an integration time of 10 s followed by immediate read out. In normal operation, readout out is initiated by a command from the ICU.

7.3 Power Card

(TBC)

7.4 Analogue Card

The block diagram figure xx shows the architecture of the Analogue Card. The two CCDs are labeled A and B, with image segments numbered 00, 01, 10, 11, in order of ascending wavelength. There are four analogue chains within the ROE, with ADC data paths which combine such that the right channels of CCDs A and B are multiplexed prior to being converted into serial data and presented to the Digital Card. The left channels are similarly combined.

The flexible PCB style cables which connect the CCD to the ROE are constructed to minimise crosstalk between sensitive signals from the CCD, to minimise capacitance to AGND, and are shielded from RFI. They are designed to be as short as is practicable so as to minimise degradation of electrode clock signals and video output signals, and to maintain a low impedance bias decoupling points on the Analogue Card.

MDM 25-way connectors with flying leads soldered into the Analogue Card connect to the flexible cables. They are mounted to the ROE housing from the inside. The connectors are specified as having stainless steel shells for robustness and RFI shielding.

The first element in each analogue chain is a low pass element which filters any susceptibility of the CCD or flexible cable to RFI, and which reduces the amplitude of clock spikes from the CCD so that the video amplifier not driven into a non-linear or saturated condition.

The baseline video amplifier is the AD859 (TBC). This has excellent input noise voltage performance of the order of 1.5 nV/Hz^{-1} To 10 kHz. Other noise sources (Johnson and shot noise) in the design are made less significant by careful choice of components in the input circuitry. The AD859 is a current feedaback amplifier with wide bandwidth (xx at a gain of 12) and correspondingly fast slew rate (xx V/μs) as required for the application.

The CDS circuits are preceded by a single pole anti-alias low pass filter with time constant ~100 ns (TBC). This may need buffering.

The CDS circuitry is a dual clamp and sample arrangement with FET buffer stages to prevent signal droop.

The ADC driver amplifier operates at unity gain and may be offset by a reference voltage of +2.5V applied to its inverting input, to produce a signal at the ADC input in the range –2.5 V to +2.5V. The +2.5 V reference is derived from the ADC in each chain. An alternative approach is to feed the $-A_{in}$ of the differential analogue input of the ADC from the +2.5 V ADC reference via a unity gain buffer.

The baseline ADC is the LT1419 (TBC). High reliability parts and radiation tolerance are being investigated with the manufacturer. In June 2000 no such parts are readily available. A low pass filter is required at the input to the ADC. The small signal bandwidth of the ADC sample-and hold circuit is 20 MHz. Any noise or distortion products which are present at the analogue inputs will be summed over the entire bandwidth. The baseline is a simple single-pole RC filter, e.g. 100 • plus 1 nF provides a pole at 1.6 MHz. The 1 nF capacitor also acts as a recommended charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch-sensitive circuitry. A high quality resistor and capacitor are recommended, e.g. metal film and NPO dielectric respectively.

When normally powered from ±5 V supplies the LTC1419 dissipates 150 mW. For 4 ADCs the total power is 600 mW, a significant proportion of the power budget. To ameliorate this the power shutdown feature of the LT1419 is be used (TBC), under control from the Digital Card. The ‘nap’ mode reduces the power by 95% and leaves only the digital logic and reference powered up.

8 EMC

8.1 System compatibility

The CCDs and ROE complies with the requirements of the spacecraft and instrument EMC requirements in respect of susceptibility and emissions, both conducted and radiated.

8.2 Grounding scheme

Complies with the requirements specified in RD3. A single point ground for connection to the instrument structure ground is provided within the ROE unit. This is made via a coaxial

connector on the rear (TBD) of the unit to enable secondary isolation measurements to be made.

Within the ROE, two possible grounding schemes are proposed. See figures xx and xx. It is proposed that the PCBs are laid out to cater for both possibilities.

AGND from the read out electronics connects to the screen of the flexible cables and to the CCD mount. The CCD mounts are electrically separate from the support structure, with an easily breakable link to connect the two.

8.3 Isolation

To comply with the overall secondary isolation requirements of the instrument, the impedances measured at the ROE with CCDs and harnesses connected shall not be outside the following limits:-

A capacitance greater than TBD nF
A resistance less than TBD M•.

To meet this overall requirement in the presence of the ICU, MHC and interconnecting harnesses, a design goal for the ROE is a capacitance of one tenth, and a resistance of ten times
The above values respectively.

8.4 Shielding

The ROE is packaged in a conductive aluminium alloy housing with no significant apertures so as to provide RFI shielding for up to ten times the RF link frequencies (~2.3 GHz). All connectors and cables shielded appropriately. The flexible cables to the CCDs are shielded with a cross hatch mesh spaced at approx 10 mm, i.e. less than 0.1 of a wavelength of the downlink carrier signal. The shields are connected to AGND on the Analogue Card and to the CCD mounts which are electrically isolated from the structure.

9 ELECTRICAL INTERFACES

9.1 Command and status link

9.2 Science data link

9.3 Power

9.4 CCD interface

9.5 Test connectors

10 COMPONENTS AND MATERIALS

11 POWER REQUIREMENTS

12 PCB AREA ESTIMATES

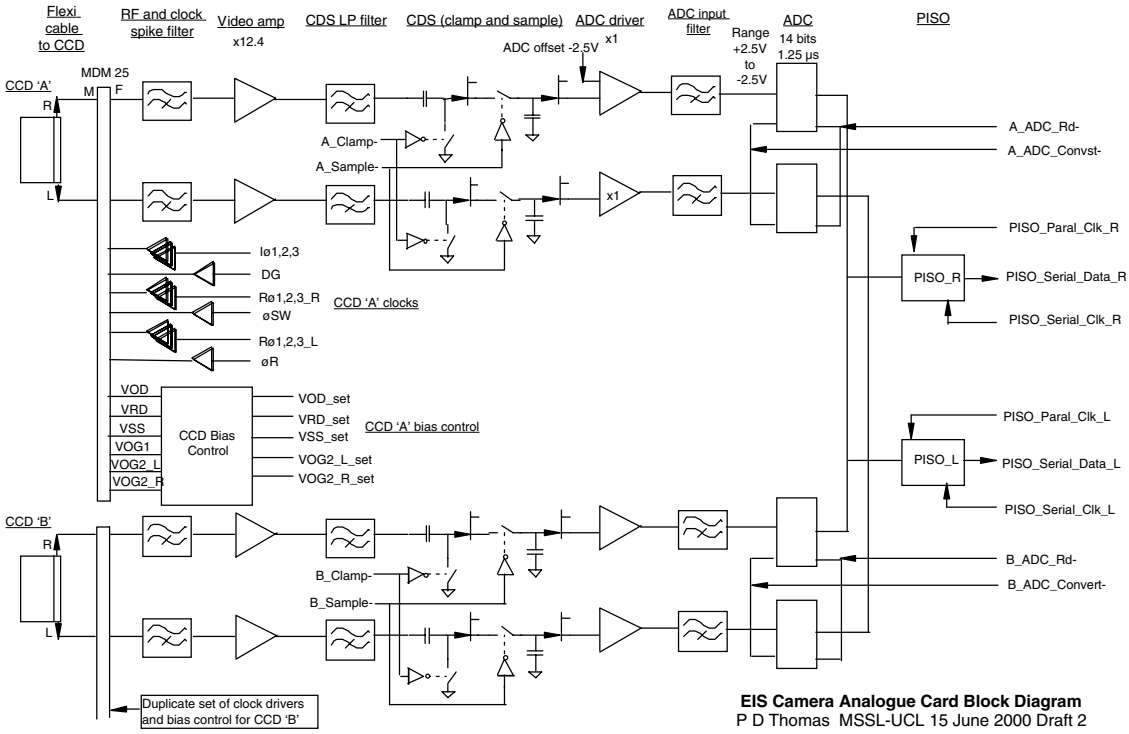

Fig. 1 Analogue Card Block Diagram

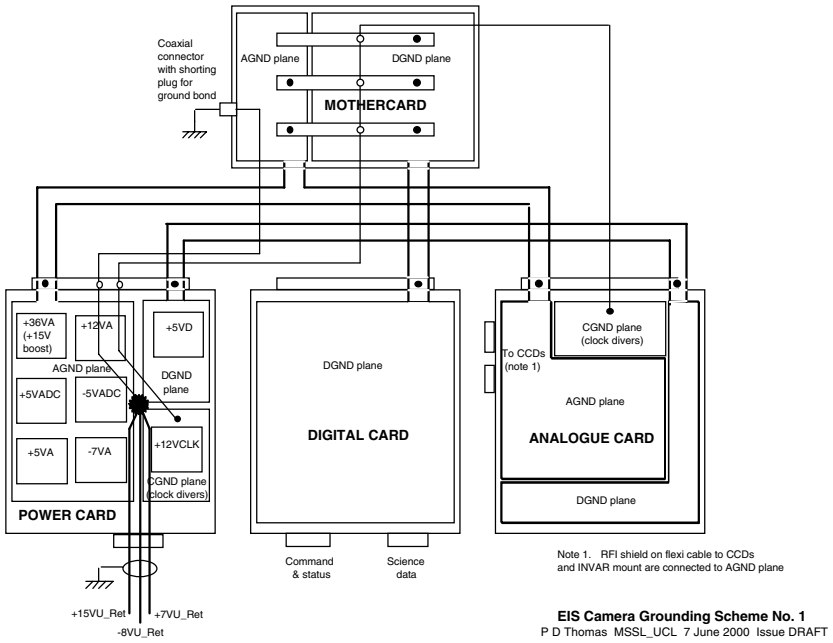

Fig. 2 Grounding Scheme 1

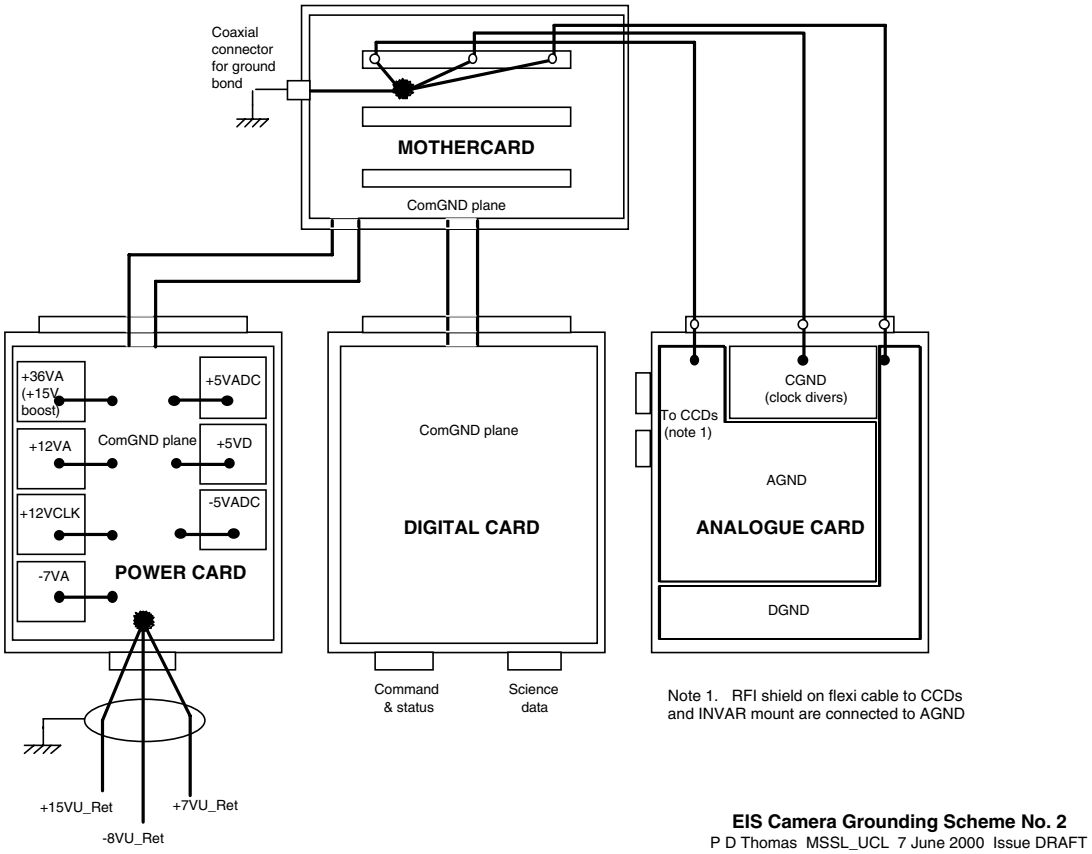

Fig.3. Grounding Scheme 2