Solar-B
EIS
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EUV
Imaging
Spectrometer

Design Requirements for the Solar-B EIS Read Out Electronics

Title	Design requirements for the Solar-B EIS Read Out Electronics
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Change Record

Date	Issue	Section	Description of change
5/06/2000	2.0	All sections	Major changes to document
25/04/2003	3.0	4.1	Delete tables one and two
		4.2.1b, 4.2.1e, 4.2.1f, 4.2.5	Requirements deleted. See ECR 116 for justification and review of these changes.

1 Introduction

1.1 Purpose

The purpose of this document is to establish the high level design for the Solar-B EIS Read Out Electronics (ROE). The system level requirements for the CCD camera (consisting of the Focal Plane Array (FPA) and the ROE is established in *MSSL/SLE-EIS/SP01* (reference [1]).

The FPA consists of two CCD chips. The actual control of the CCD itself, such as generation of the appropriate clocking signal, and the measurement and digitisation of the CCD analogue output will be the responsibility of the ROE. The top-level design requirements for CCD control and measurement through the ROE are specified in this document.

1.2 Abbreviations

CCD Charge Coupled Device

CTE Charge Transfer Efficiency

EIS Extreme Ultraviolet Imaging Spectrometer

FPA Focal Plane Assembly

ICU Instrument Control Unit

ROE Read Out Electronics

1.3 Applicable Documents

AP1 EIS CCD Camera - Systems Requirement Document - MSSL/SLB-EIS/SP01

AP2 Solar-B EIS ICD Document - MSSL/SLB-EIS/SP003

1.4 Referenced Documents

RD1 Possible charge injection method. P. Pool, Marconi. Personal communication. December 1999.

2 Definitions

Frame - one CCD image, i.e, all the charge collected from the start of the integration period, to the end of this period which is subsequently then downloaded to the ICU.

3 ROE design requirements

3.1 Important CCD features

- The Marconi 42-20 devices are full frame devices, with 2048 imaging pixels in the spectral direction and 1024 pixels in the spatial direction. In addition, in the serial register between the imaging pixels and each amplifier there are an additional 50 pixels which are covered with Aluminium and are not sensitive to light but can be used for calibration purposes. In total therefore, there are 2148 pixels in the serial register;
- Backthinned to maximise quantum efficiency;
- Three phase clocking with minimum row shift ~8μs to overcome vertical electrode capacitance, and minimum pixel shift ~2μs (TBC);
- Used in MPP mode to minimise the thermal noise;
- There are two read out ports, one at each end of the readout registers. Charge will be clocked down rows in the spatial direction and read out in the spectral direction.

4 ROE specification

4.1 ROE circuitry

4.1.1 Master Reset

It shall be possible to reboot the ROE using a master reset (4.1.1a), initialising the registers to the default values and returning the ROE to the continuously running mode.

4.1.2 Clock speed - TBD

4.1.3 ADC Resolution

The full well capacity of the CCD at the long wavelength range corresponds to about 7500. Consequently, **the ADC resolution shall be 14 bit (4.1.3a)**. *The amplifier gain will be set slightly above 5.5 electrons/DN (4.1.3b)* to leave 'spare' dynamic range available to cope for small amounts of ADC drift over time.

4.1.4 Time for correlated double sample

Due to the photoelectric effect, an incident photon will be converted into a number of electrons. At the short wavelength range (170Å) one photon will generate about 20 electrons, and at the long wavelength range (290Å) one photon will generate about 12 electrons.

The minimum signal detectable by the CCDs will be 1 photon, which will correspond to 12 electrons at the long wavelength range. Thus, the minimum "shot" noise on the detected

signal will also correspond to 12 electrons (i.e one photon). To maximise the signal-to-noise ratio, the quantisation noise and read noise values should be below the signal shot noise. However, the rms addition of these terms means that there is very little advantage in having quantisation or read noise values which are substantially below the photon shot noise.

The thermal noise generated at the expected CCD operating temperature (about -55°C) will be minimal except for very long integration times, and will then still be significantly below the signal shot noise.

An amplifier gain of slightly above 5.5 electrons/DN will ensure that the quantisation noise is well below the signal shot noise.

Using the figures in the Marconi 42 series data sheet, a readout noise of around half the signal shot noise corresponds to about 6 electrons rms, and this corresponds to a readout time of around 2μs per pixel. Consequently, **a clamp and sample rate sufficient to allow a readout rate of 2μs per pixel shall be adopted (4.1.4a).** *To achieve this figure, a low pass filter will be required with a time constant of order 100ns.*

4.1.5 Dump charge using the dump drain/flush the CCD

To maximise the CCD readout rate (i.e the temporal resolution), a dump drain is provided with the 42 series CCDs allowing unwanted rows to be quickly dumped.

It shall be possible to quickly dump charge from the CCD using the dump drain provided (4.1.5a).

It shall be possible to dump a single line of the CCD; multiple lines; or the entire CCD (4.1.5b).

It shall be possible not to flush the CCD before each image (4.1.5c).

4.1.6 Read out to left/right amplifier or both simultaneously

To maximise the readout rate for each CCD, **it shall be possible to specify whether the charge read out is to be from the left hand amplifier, the right hand amplifier, or both (4.1.6a).**

4.1.7 Programmable features:

The following values **shall** be programmable within the ROE:

a **CCD clocking rate (TBC) (4.1.7a)** The intended time to read out each pixel is 2μs. If possible, it should be possible to clock unwanted pixels within a row (i.e. those outside a window) through the CCD at 1μs per pixel to maximise the read out rate.

b **Phases held high during integration (e.g IØ1 or IØ1/IØ2) (4.1.7b)(TBC)** as the quantum efficiency of the CCD may vary depending the number of phases held high during integration;

c Voltages applied to **V_{RD}, V_{OD} and V_{SS} over a range of 4 volts with 16 steps (i.e, ¼ volt) being used (4.1.7c)** to minimise any flat band voltage shifts due to ionising radiation.

4.2 Imaging modes

4.2.1 Window read out

To increase the CCD readout rate, on chip-windows shall be available.

It shall be possible to select a known area of the image in the form of a rectangular window (4.2.1a) (i.e region of interest). Charge from pixels prior to the read out window, and after the read out window, do not need to be read and can be quickly dumped.

Windows shall be capable of being any width (within the half of the CCD) and height (4.2.1.b) but, for any single image, both windows on the CCD shall be the same height and width (4.2.1.c).

It is important to minimise the noise in the ADC process, particularly cross talk between CCDs. For example, clocking out one CCD during digitisation of a pixel on the second CCD could lead to substantial noise through cross talk. Consequently, it would not be advisable to quickly clock out pixels on one CCD containing no relevant data whilst pixels on the other CCD were being digitised, as this would lead to significant noise. In that case, all pixels will be clocked out at the same rate.

Thus, the two ways to minimise cross talk are:

1. The window heights on both CCDs will be the same so that all vertical clocking can be simultaneous.
2. The window width will be the same on both CCDs. This is explained in figure one. Although the potential width of the window for both CCDs could be different, the overall readout times of both CCDs (which will control the cadence) is dependant on the widest window width. Consequently, the electronics design will be simplified if the window widths are the same.

It must be remembered that there are 50 non imaging pixels at both ends of the serial register. That is, to read out pixel 0 from the image, it will first be necessary to read out 50 pixels from the serial register.

4.2.2 Binning in the serial and parallel registers

Hardware binning of any number of pixels, in both the spatial and spectral directions shall be available (4.2.2a).

Binning can be implemented in the spatial direction by clocking more than one row into the serial register before clocking out the charge in the serial register.

Binning in the spectral direction can be implemented by suppressing the reset pulse to the output amplifier when clocking a charge packet onto the amplifier.

The serial register in the Marconi 42-20 CCD chip allows up to 300k (i.e 15k photons at the short wavelength range) electrons to be binned in before non-linearity appears. However, in some circumstances this value may not be sufficient for EIS. Consequently, **it shall be possible to enable the low responsivity amplifier mode if required (4.2.2b).** In this mode the voltage on the output gate OG2 is increased to 20V, and the responsivity of the CCD output amplifiers is reduced such that up to 540k electrons (27k photons at the short wavelength range) can be binned into the serial register before amplifier non-linearity begins to occur.

4.2.3 Integration and readout

In normal use, the integration period will be controlled by the ICU, which will command the ROE to begin clocking out the CCDs at the end of the integration period. The sequence of commands from the ICU to the ROE during a normal integration is shown in figure one.

Upon power up, the ROE shall have a default mode of operation in which it continuously clocks out the CCDs every ten seconds (4.2.3a). This default mode of operation ensures that images will still be available from the ROE even if it is not possible for the ICU to control the integration time via the low speed command link. Upon power up, the ROE will operate in the default, continuously imaging mode of operation. However, in normal use, the ICU will command the ROE to disable this mode.

Commands from the ICU to the ROE **shall** be used to:

a **Disable the continuous running mode (4.2.3b)**, allowing full control of integration time by the ICU;

b **Flush the CCD (4.2.3c)**;

c **Update any new register values which have been sent from the ICU during integration (4.2.3d);**

d C**lock out the CCD (4.2.3e);**

e **Indicate the end of frame (4.2.3g).**

4.2.4 Overclocking

Overclocked pixels can be used to assess the CTE from the CCD, and to determine the ADC bias value. The 42 series CCDs have 50 'lead-in' pixels at each end of the serial register which have to be clocked through the output amplifier before the first pixels containing image information are measured. **It shall be possible to obtain additional, non-imaging pixels by 'overclocking' pixels within each row (4.2.4a)** (i.e. continuing to clock and read charge in the output amplifier after the last lead in pixel has been read). As 12 bits are available to specify the row coordinates there will be a maximum of 4096-2048-100 = 1898 pixels available for overclocking (at most about 50 would be expected to be used).

In addition **it shall also be possible to overclock the CCD in the spatial direction (4.2.4 b)** (i.e, creating "virtual" rows). Thus, the register value which contains the number of rows to clock must be large enough to handle 2048 rows.

4.2.5 Test Ports

Test ports shall be available to allow testing of the ROE via an external EGSE (4.2.7a), without using the ICU. In addition, several test points may be provided to allow the analogue CCD signal to be viewed from each port without the need to download images via the ICU.

4.2.6 Stim Patterns

i **It shall be possible to inject a known image pattern into electronic front end, immediately after the CCD preamplification (4.2.8a)**, so that this image can then be clocked out to determine how the image may be degraded by the readout process;

ii **A stim generator shall be built into the ROE logic (4.2.8b)** to allow precise identification of specific pixels.

4.3 Other modes

4.3.1 Thermal control

A combination of a passive radiator and resistive heating must be provided to keep the operating temperature of the CCD within its defined limits and to permit heating of the CCD to allow evaporation of any contaminants.

Minimum temperature required: -55°C

Maximum temperature required: +30°C

Range within which temperature is maintained: ±2°C (TBC)

Maximum allowable heating or cooling rate: ±10°C/minute

5 CCD bias requirements

CCD bias voltages for each pin are described in table 2.

6 Power Distribution

6.1 Requirements

The CCD and ROE shall be powered off together.