Technical note

Comments on temperature sensitivity of Solar-B EIS CCD dark levels and signal amplitude

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Reference documents

1. Solar-B/EIS CCD readout characteristics, Dave Pike, RAL, 23-Aug-2004
2. Solar B-EIS Readout Electronics: Analogue Design Specification MSSL/SLB-EIS/SP010.05

Introduction

This technical note is a response to Dave Pike's memo of 13-Aug-04 (Ref. 1), in which he summarises the EIS CCD readout characteristics obtained from data taken at RAL as part of the EIS FM calibration. The data he obtains for system read noise and responsivity are consistent with measurements of the FM at MSSL using Dave Walton's CCD light transfer characteristic (LTC) analysis software.

It is worth noting that the sensitivity of the dark level shift with CCD temperature is of the order of 120 ppm/ºC and is not dependent on ROE temperature, whose temperature will in any case be relatively stable in orbit. The variation of CCD output sensitivity with temperature is a more significant issue, being of the order of -1000 ppm/ºC. In my opinion, the gain vs. temperature of the EIS spectral amplitude will be the greater issue for the science team to contend with.

During operations it may be necessary to take reference dark images at various stages of the orbit, in accordance with CCD temperature. It should be noted however that the resolution of the CCD temperature monitors is 2 ºC, which is fairly coarse.

After further analysis of other data and tests on the PFM camera the most likely causes of dark level (ADC bias) shift are a combination of:-

1. Temperature variation of CCD output amplifier sensitivity.
2. Feedthrough of the readout clocks within the CCD into the CCD output signal, and insufficient settling time of feedthrough spikes.
3. Temperature variation of clock feedthrough energy.

MSSL data analysis

Listed below are measurements made by MSSL at RAL prior to and during the EIS AIT operations. The LTC software analyses data from only CCD B (CCD areas 1 and

2). The measurements shown in Table 1 are the average of 5 data sets, however the instrument configuration was not fully representative of the FM. Connector saver pigtails were fitted to the CCDs, which could account for the increase in noise level and shift in dark level. The results shown in Tables 2 and 3 were obtained during AIT at RAL with the instrument in its flight configuration, with savers removed.

Dave Walton confirms that the poor repeatability of the system responsivity measurement is due to the low illumination levels applied. In some cases no external illumination was used; only the increasing dark current during the readout at ambient was present.

The dark levels shown in Tables 2 and 3 compare well with those of run 168 listed in Dave Pike's memo. However in obtaining the data sets it is likely that the CCD cooling had not stabilised before a particular series of measurements was taken.

The dark (ADC bias) level is the difference between the CCD reset level and the dark video level. This is sensitive to change of gain of the CCD output amplifier. The RAL measurements agree with those of MSSL in that in the worst case (CCD area 4) the temperature sensitivity of the dark level is ~ 2 DN/°C, i.e. ~120 ppm/°C.

CCD area	*CCD Port ID*	*Responsivity e-/DN (avg.)*	*Noise e- RMS (avg.)*	*Dark level DN (avg.)*
1	BL, 3	5.84	13.8	525
2	BR, 2	6.08	13.9	434

Table 1. Initial set up, 23-Jan-04. Run 67, files 7- 21, avg. of 5 data sets.

CCD area	*CCD Port ID*	*Responsivity e-/DN*	*Noise electrons RMS*	*Dark level DN*
1	BL, 3	5.70	12.8	550
2	BR, 2	5.90	12.6	464

Table 2. During AIT at RAL, 13-Feb-04. Run 87, files 5-7.

CCD area	*CCD Port ID*	*Responsivity e-/DN*	*Noise electrons RMS*	*Dark level DN*
1	BL, 3	5.20	9.86	546
2	BR, 2	5.61	10.2	454

Table 3. Pre-vibration, 22-Mar-04. Run 107, files 7-9.

Variation of CCD output sensitivity with temperature

All CCDs display a variation of output sensitivity with temperature, owing to the increased carrier mobility and forward transconductance of the on-chip FET amplifiers at lower temperatures. The E2V test data for the EIS FM CCDs quantifies the output sensitivity, which is an order of magnitude greater than the observed variation of dark level with temperature in the EIS data.

The deliverable test data from E2V for the FM CCD performance measured at 20°C and -60°C indicates an increase in output amplifier gain of about 8% at the lower temperature, with the FET current at 5 mA, i.e. -1000 ppm/°C. As an example, the measured output sensitivities for CCD 0043-02-04 are shown in Table 4. The figures are consistent with the typical gain variation of E2V CCDs which incorporate a two-stage MOSFET output amplifier.

Analysis of data from run 156 by Matt Whillock clearly demonstrates the relationship between CCD temperature and dark level. The ROE was isothermal throughout the measurement.

℃	*left port μV/e-*	*right port μV/e-*
20	3.80	4.02
-60	4.07	4.39
ppm/°C	-890	-1150

Table 4. Variation of output sensitivity with temperature of EIS FM CCD 0043-02-04

Settling time of CCD video output signal

In an attempt to eliminate the cause of shift in dark level being related to the settling time of the CCD output signal, we referred to a series of measurements made on 24-Feb-03 with a set-up grade CCD. In order to minimise dissipation in the CCD, the EIS camera was designed to supply a 2 mA bias current to the CCD output FET, this current being slightly less than the range 3 to 5 mA recommended by E2V. The camera was set up and tests were performed with the FET currents set at 2 mA for the left port and 5 mA for the right port. The results are summarized in Table 5.

CCD B port	*Video fall time constant to 60%*	*Video settling time to 14 bits*	*Reset rise time to 90%*	*Rise time to reset peak*
Left, I_{FET}=2 mA	60 ns	9.7 x 60 = 582 ns	50 ns	110 ns
Right, I_{FET}=5 mA	50 ns	9.7 x 50 = 485 ns	40 ns	100 ns

Table 5. Summary of video CCD output responses for output FET currents 2 mA and 5 mA

In the ROE the ADC conversion starts 750 ns after the start of the video signal, so there is a margin of at least 150 ns in settling time in the case of the signal from the CCD left port with 2 mA FET current. It is therefore unlikely that the settling time of the video signal contributes to the change in bias level.

The CCD video output signal passes through several stages of filtering in the analogue signal chain, to reduce the amplitude of clock spikes and filter unwanted RF, low pass filter prior to the correlated double sampler, and ADC input filter. The combined settling time of these filter stages is less than 750 ns.

Settling time of feedthrough of readout clocks

Suppose that within the CCD there is a temperature variation of the amplitude of feedthrough spikes of the readout clocks coupled into the CCD output signal. This could simply be due to a variation with temperature of output sensitivity and possibly due to a variation of rise/fall times of the CCD output amplifier, but may also be due to a change with temperature of the resistance of the readout electrodes.

A problem would occur if the settling time of the low pass filters in the analogue signal chain were slightly longer than required for the clock feedthrough to settle during either the reset or video phases of the correlated double sampling. This would manifest as a variable offset in the measured difference between the reset level and the video level.

The above problem could be exacerbated in case of the EIS clocking scheme. It was necessary to adopt an unconventional clocking scheme for EIS due to the requirement to use a relatively slow ADC, the LTC1419, on account of its radiation tolerance (Ref 2, 7.3.4.3). There was also a requirement not to toggle the CCD clocks during the ADC conversion period to reduce the possibility of switching currents in the signal ground causing errors in the 14-bit conversion.

The conversion period of the LTC1419 is 1.25 μs, which is greater than half the pixel period of 2 μs. In the EIS scheme, after Rφ3 has clocked out a video signal, both Rφ1 and Rφ2 are cycled and Rφ3 toggled to its original state, completing a full clock triplet, before the ADC conversion is started. This is to minimise the risk of digitisation errors. A temperature variation in amplitude of the clock feedthrough would cause a problem is the settling time was insufficient.

Kerrin Rees has suggested that the above theory could be tested relatively easily by uploading a number of experimental horizontal clocking schemes to the ROE and comparing the dark levels at various temperatures, say, from -20 to -50 ºC. This could be tested on the spacecraft. A new clocking scheme could be stored in E^2PROM within the ICU, and uploaded to the ROE, subject to a change of flight software.

By rearranging the clocking scheme it might be possible to significantly reduce or even eliminate the effect of clock feedthrough without increasing the pixel period 2 μs (500 kpix/s) or degrading other performance parameters. However it might be found that the pixel period needed to be slightly increased to 2.25 μs (444 kpix/s) or 2.5 μs (400 kpix/s). In the worst case 3 μs (330 kpix/s) would probably be the slowest speed required.

Recent tests on the PFM camera

Recent tests with the PFM camera and set-up grade and EM CCDs have shown no significant difference in output sensitivity of the CCD employing both 2 mA and 5 mA output currents at the left and right ports. However it may be that at the 2 mA current the output FET is biased less optimally than at 5 mA. A discussion with E2V should easily resolve this question.

Measurements were also made on the PFM of the difference between the reset level and dark video level voltages at the CCD outputs, using both set-up grade and EM CCDs at 25 ºC. At this temperature, differences of only a few percent were observed on each of the four channels, which is probably mainly attributable to dark current. This suggests that the dominant cause of the dark level variation is not the small step between the reset level and the dark video level. The evidence points to some other mechanism such as the variation in output sensitivity convolving with readout clock feedthrough.

The ROE signal chain gain stability and dark reference level applied to the ADC were also checked. Both were stable to better than 25 ppm/degC, with the CCD temperature at a constant 25 ºC, and ROE temperature varied from +25 to +75 °C, thus eliminating the ROE as a contributor to the stability of signal gain and DC bias level in relation to the CCD.

Possible further work

In Japan, supported from MSSL:-

1. Investigate modified horizontal clocking schemes and the possibility of trading off pixel rate against dark level temperature sensitivity.
2. Repeat system noise and responsivity measurements using Dave Walton's LTC software with flat field illumination to produce a near full-range of exposure during readout (after 0 s exposure).

At MSSL:-

1. Obtain from E2V the CCD42 output FET characteristics so that the DC operating point can be further assessed.
2. Discuss with E2V the possible causes of variation of readout clock feedthrough with temperature, e.g. change of resistivity of Rφ electrodes.
3. Perform further analysis on instrument calibration data.

During in-orbit operations:-

1. Possibly take reference dark images at various stages of the orbit, in accordance with CCD temperature, and subtract from image data.
2. Possibly modify the EIS spectral amplitude to take into account the variation of CCD output sensitivity with temperature.