Solar-B **EIS** * EUV Imaging Spectrometer	CCD power requirements for Solar-B

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Doc ID	MSSL/SLB-EIS/TN/007
ver	2.0
Author	Chris McFee
Date	27 October 2000

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Chris McFee, 23/2/1999

Change Record:

27/10/2000 Update power levels for 500kHz read out and the increased capacitance on an MPP device

This short memo provides a summary of the expected power dissipation associated with the CCD. There will be three major components for the power dissipation: the on-chip power dissipation due to the charge being repeatedly clocked through the CCD substrate; the power dissipated by the clock drivers in providing the necessary voltage clocking to actually drive the CCD; and the power dissipated during charge integration. Overall, the on-chip dissipation of power should be very low (of the order of 25-50mW or so) until TV frame rates (i.e, almost continuous clocking of the parallel transfer section) are reached.

The power dissipated on-chip is given in [1] as

$$P \sim C^2 V^2 f^2 R_S PI^2/2.$$

where C is the capacitance of each three phase pixel, V is the clock voltage swing, f is the clocking frequency, and Rs is the electrode series resistance.

Typical values for an EEV 42-10 (taking values from the 42-10 data sheet and the EEV circuit equivalent diagram) operated continuously are:

C = 8nF (i.e ~2nF per phase), V=12V, f=.5MHz (i.e 2us per clock), Rs=23,

This gives an on-chip power dissipation of ~260mW

Using representative values for the EEV-42 CCD series, and using representative clocking rates yields the following:

CCD type	C (nF)	Rs (Ohms)	f=150khz	f=330khz	f=500khz
42-10	8	23	23mW	113mW	261mW
42-20	9	18	16mW	112mW	260mW
42-20 (MPP)	22	18	180mW	674mW	1.5W
42-40	14	20	65mW	303mW	700mW
42-80	28	32	400mW	1.9W	4.4W

Total power dissipated by the clock drivers

This is given (in both [1] and [2]) as $P=fCV^2$

where C is the capacitance (3nF) and V is the clock pulse amplitude (12V)

hence P= 576mW for a 42-10 clocked at 500khz. This is the maximum power dissipation that could be expected, i.e assuming 100% duty cycle.

Typical power dissipations to be expected are

CCD type	C (nF)	f=150khz	f=330khz	f=500khz
42-10	8	172mW	380mW	576mW
42-20	9	190mW	427mW	648mW
42-20 (MPP)	22	475mW	1W	1.6W
42-40	14	300mW	665mW	1W
42-80	28	600mW	1.33W	2W

Quiescent power dissipation

There will also be a quiescent power dissipation (given by VI) associated with the clock drivers during image integration. In total, there will be a number of clock drivers each contributing to the quiescent power dissipation. Two drivers are required for each parallel phase, one for each reset gate, one for each readout phase, and one for the dump gate (which will, however, usually have a lower duty cycle than the other drivers). The typical dc current drawn is around 7mA, this leads to a typical power dissipation as follows:

parallel phases - 3x12x7 = 252 mW

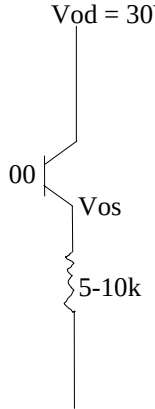
Left serial phases and reset - 2x11x7 = 154 mW

Right serial phases and reset - 2x11x7 = 154 mW

dump gate - 1x7 = 77 mW

Thus, the typical quiescent power dissipation is around 650 mW.

In addition, the on-chip output node FET will also draw current. The output FET is shown below:



For each output, (Vod-Vos)xI = 12 mW will be dissipated to the CCD

and (Vos x I) = 168 mW is dissipated through the load resistor into the FPA.

Power dissipated by the readout electronics

The figures I have for the readout electronics come from Dave Walton and are "typical" figures for the Integral readout electronics, powered by desk top power supplies. During integration, the power dissipation of the ROE (including ADCs) is about 4 W, during clocking it is about 4.2 W.

References

[1] - CCD performance limitations: theory and practice. D J Burt

[2] Charge coupled devices and their applications. J.D.E Beynon and D. R. Lamb