Solar B - EIS

MULLARD SPACE SCIENCE LABORATORY
UNIVERSITY COLLEGE LONDON **Author: K. Al-Janabi**

EIS Status

Document Number: MSSL/SLB EIS/SP017.06

Distribution:

Author	K. Al-Janabi	Date:	20/06/2005
Authorised By	A. James	Date:	20/06/2005
Distributed	A. Spencer	Date:	20/06/2005

EIS-Science	✓
EIS-Tech	✓

CHANGE RECORD

ISSUE	DATE	PAGES CHANGED	COMMENTS
01	08/12/2000	All new	Draft release
02	12/06/2001	6 6 9 11 11	Define TC_FAILED_EC values Removed TC_EXC_PKTC (not needed, spare parameter) Added ICU ERROR Flags Added last CMD sent parameters [8] Added ICU/MDP hardware interface statuses
03	09/12/2002	6 12 17 20	Updated ICU status parameters Updated PSU status parameters [10] Updated CAM status parameters [11] Updated MHC status parameters [4]
04	18/12/2003	6 21 25	Updated ICU status parameters Updated CAM status parameters Updated MHC status parameters
05	05/08/2004	10 13 25 26 34	Sequence number and length are 128 * 128 Added MDP data compression error status Added EIS event trigger status parameters Various corrections in MHC clamshell status Corrected ICU watchdog timeouts according to NCR-19
06	20/06/2005	Various 8 10 12 13, 22 13 15 15,16 27	Clarified issues raised, NCRs and ECRs changes Corrected an error in CCDs buffer test Updated FMIR position reporting in line with FM SW Added EEPROM MHC code load status Added BO closed loop heater controller status parameters Updated MDP Line List error reporting in line with the new MDP requirements Added internal EEPROM copy status parameters Added AEC error status parameters Updated the MHC status in line with [4]

LIST OF CONTENTS:

Glossary and Convention:

ADC	Analogue to Digital Converter
AE	Camera Analogue Electronics
AEC	Automatic Exposure Controller
BC	Block Command, Solar-B Command parameter
BO	Bake Out
CAL	Calibration
CAM	Camera
CMD-ID	Command ID
CMIR	Coarse Mirror
DC	Discrete Command (Solar-B use)
EIS	Extreme-ultraviolet Imaging Spectrometer
EOF	End Of Frame
ET	Event Trigger
FMIR	Fine Mirror
FOV	Field Of View
FT	EIS internal Flare Trigger
GRA	Grating
GSE	Ground Support Equipment
HSL	EIS Camera High Speed Link
ICD	Interface Control Document
MD	Mission Data (Solar-B Science packets)
MHC	Mechanism and Heater controller
MMH	MHC Message Header
N/A	Not Applicable
OCB	On Chip Binning (CAM function)
OOL	Out OF Limit
Reg.	Register
PSU	Power Supply Unit
ROE	Camera Read-out Electronics
SLA	Slit/slot subassembly and includes the shutter
SS	Slit/slot mechanism
TI	Time Indicator (calibrated MDP time as maintained by the ICU)
VOD	CCD Voltage Output Drain
VOG	CCD Voltage Output Gain
VRD	CCD Reset Drain voltage
VSS	CCD Substrate voltage
QCM	Quartz Crystal Microbalance (contamination monitor).

Applicable references:

These references appear in [] brackets in this document.

1 – EIS Science requirements: MSSL/SLB-EIS/SP007.07
2 – MDP ICU interface document: NAO/SLB-EIS/SP/MDP3.4
3 – EIS Mode definition: MSSL/SLB-EIS/SP0013.03
4 – MHC software ICD (ICU-MHC), Version 17.1.
5 – CAM Commanding and HK. Email from K. Rees on the 16th Nov. 2000
6 – PSU Commanding and HK. Email from A. McCalden on the 17th Nov. 2000
7 – EIS Telecommanding: MSSL/SLB-EIS/SP0016.06
8 – Working meeting at MSSL with ISAS/NAOJ between 26-28/03/2001.
9 – Back-plane definition
10 – New PSU status list received on the 31st May 2002
11 – New CAM status list received on the 29th August 2002
12 – Solar B-EIS heaters and temperature sensors: MSSL/SLB-EIS/TN/0016.06
13 – ICU Closed loop bake out heater controller: MSSL/SLB-EIS/TN033.01
14 – EIS Health Monitor (auto safe): MSSL/SLB-EIS/SP052.02
15 – Automatic Exposure Control (AEC) for EIS: MSSL/SLB-EIS/SP027.03

1.0 Introduction:

This document outline EIS status parameters, to be flown on Solar-B satellite.

Note that within this document and in compliance with Solar-B S/C requirements, Bit 0 is the Most Significant Bit. Also note that all the status data parameters are unsigned unless otherwise stated.

2.0 Solar-B Status data Structure:

Status data packets (instrument HK) consist of a 4 byte header followed by up to 2 Kbytes of status data [2]. The general format is as follows:

Header Area		**Data Area**
Data Type	Packet Size	Status Data
8 bits	24 bits	Max. ~2 Kbytes

The following are the EIS status allocations:

Type 1: ICU status, including the PSU status (2 seconds acquisition)

Header Area		**Data Area**
Data Type	Packet Size	EIS Status type 1 Data
8 bits	24 bits	100 bytes

Type 2: Type 1 + CAM status (10 seconds acquisition)

Header Area		**Data Area**	
Data Type	Packet Size	ICU Status type 1 Data	CAM status
8 bits	24 bits	100 bytes	150 bytes

Type 3: Type 1 + MHC status (10 seconds acquisition)

Header Area		Data Area	
Data Type	Packet Size	ICU Status type 1 Data	MHC status
8 bits	24 bits	100 bytes	150 bytes

The following table shows EIS sub-system allocations:

Subsystem	**Allocation in Bytes**	**Comments**
ICU	100	Include PSU
CAM	150	Include additional ICU status parameters (slow changing parameters)
MHC	150	

2.1 ICU Status:

For the ICU status, there are 100 bytes allocated, including key PSU parameters. Note that the spare fields will be allocated in the future.

Because the MDP acquires status data asynchronously from the ICU, the first status packet may not be valid (invalid acquisition bit is set) following a re-boot, also the last packet before a reset may be invalid as there is a small possibility that a reset may take place while a packet is actively being transmitted.

Byte No.	Name	Description	Range
0	ICU_SW_ID	The ICU software version ID. Each software release has a unique identifier	Bit 0 – 3: Version ID Bit 4 – 7: Version sub-ID Ex: ICU_SW_ID = 0X12 means SW version 1, release 2
1	EIS_MODE	The ICU present mode [3]. This is a 4-bit parameter.	Bit 0 – 3: EIS modes values 1 = STANDBY 2 = MANUAL 3 = AUTO 4 = BAKE_OUT 5 = EMERGENCY
1	TC_FAILED_EC	Last TC packet failed to execute error code. This is a 4-bit parameter. Commanding overload means that the ICU software TC buffer is full. Mode transitions not allowed means that CMD-ID = 0x20 has not been sent [7]. Incorrect mode transition means that new mode requested is rejected (e.g. change mode from standby to Auto) [3]. Command FIFO error means that the ICU read a full TC packet without detecting the end of the TC packet envelope (ICU H/W internally generated flag). Incorrect mode of operation means that the required operation cannot be performed from this mode. For e.g. sending a command to the MHC when in Standby mode (the MHC is OFF). EEPROM magic number table error (**bootstrap only**) indicates that the EEPROM control parameters are corrupted and the application software cannot be executed. Verify EEPROM contents via memory dump. EEPROM enable error indicates that the access inhibit remains active while an access (read-write) is attempted. This is a result of	EIS Error Code: Bit 4 – 7: EIS Error Code defined up to date are as follows: No error = 0 Incorrect no. of parameters = 1 Commanding overload = 2 Incorrect mode transition = 3 Mode transitions not allowed = 4 Unknown CMD-ID = 5 Operation not supported = 6 Out of range = 7 Command FIFO error = 8 Incorrect parameter value = 9 Incorrect mode of operation = 10 EEPROM magic number table error = 11 EEPROM enable error = 12 EEPROM programming error = 13 EEPROM disable error = 14

Byte No.	Name	Description	Range
		hardware error. EEPROM programming error means that a page programming error occurred. This error is logged if the read back values do not match the written values (software detected error). EEPROM disable error means that the access inhibit bit is not asserted when the EEPROM is put in reset state. This is a result of hardware error. This is a serious error that may result in loosing the EEPROM content in the event of power glitch or switch OFF. In order to recover (putting the EEPROM back reset), send an EEPROM memory dump command (single byte) and monitor the reset line via byte 38 (EEPROM status after access). Consult a member of EIS team. Note that when the ICU operational code starts, the ICU ensures that the EEPROM is in reset state and if failed, then this error code is generated and CMD-BC1 (byte 14) is set to zero to indicate that the failure is not a result of ground commanding. Other error code values are self-explanatory CMD BC1 = 0x23 is required to resets the error bits to 0.	
2 & 3	STATUS_PC	Status packet counter. This parameter is a 16-bit counter. This counter is initialised to 0 upon the ICU starting up and incremented by 1 for each status packet sent to the MDP.	0 to (2^16 –1)
4, 5, 6 & 7	MDP_TIME	This is a 32 bit parameter which indicates the status packet acquisition time (MDP time)	0 to (2^32 –1)
8 & 9	TC_REC_PKTC	TC packets received counter. This is a 16-bit counter. This counter is initialised to 0 upon the ICU starting up and incremented by 1 for each TC packets received. This counter excludes status and memory dump requests (MDP autonomous requests).	0 to (2^16 –1)
10	CMD_IF_ERROR	These flags are set to 1 if an error is detected in the MDP-ICU command interface. Bit error indicates an error in TC packet transmission occurred (bytes should be multiple of 8-bits). Spurious interrupt means that an interrupt is generated by the hardware which is not related to a command transmission completion (e.g. glitch) FIFO overflow means that the command hardware buffer has more the 4Kbyte (shouldn't happen). Bits 3, 4, 5 and 6 are related to the hardware	Bit 0 to 7: Command interface Error flags Bit 0: Bit error Bit 1: Spurious interrupt Bit 2: Command FIFO overflow Bit 3: Missing end of command marker Bit 4: End of command marker mismatch Bit 5: Command FIFOs bytes Mismatch Bit 6: Command FIFOs bytes error Bit 7: Spare bit

Byte No.	Name	Description	Range
		command FIFO [9]. Due to the relatively low SEU tolerance of the command FIFO, incoming command bytes are written to 3 FIFOs, in parallel. The ICU software uses a voting technique if an error is detected. Any error detected is reported in these 4 bits. Bit3 indicates that no end of command marker is detected in an incoming command. Bit 4 indicate that only 2 of the 3 end of command marker are matched, i.e. one marker is missing (SEU). Bit 5 indicates that one of a 3 command bytes is corrupted Bit 6 indicated that none of the 3 command bytes are matched. This will result in resetting the command interface. CMD BC1 = 0x23 is required to resets the error bits to 0.	
11	CCD_BUFF_TEST	These two bits indicate the status of CCD buffers testing. These bits are set in response to command BC1 0x8b (TEST_CCD_BUF) Note that if bit 1 is set, then the first address and the total number of memory locations failed are reported in bytes 44 to 51 of the CAM status (status type 2). The test consists of two parts; write/read a specific pattern whereby each memory location write is followed by read and compare, and the second part is read and compare pattern (data retention). If an error in encountered in the first part, then bit 2 is set. If an error encountered in part two, then bit 3 is set (data retention problem). Note: Bits 0 to 4 are automatically reset to zero when a new test starts.	Bit 0: CCD buffer testing status 1 = Test in progress 0 = Idle Bit 1: CCD buffer test error 1 = A memory test error occurred 0 = Test OK. Bit 2: Memory write/read error 1 = A memory test error occurred 0 = Test OK. Bit 3: Memory read only error 1 = A memory test error occurred 0 = Test OK.
11	PSU_STAT_ERROR	These bits specify the reasons for PSU status invalid flag. The ADC error flag indicates that the ICU has timed out while waiting for the ADC conversion completed flag (10 ms time-out). The PSU marker flag indicates that the ICU couldn't locate the start of the PSU status table. CMD BC1 = 0x23 is required to resets the error bits to 0.	Bits 4 to 5: PSU status error flags Bit 4: ADC error flag Bit 5: PSU marker error
11	ET_STAT	Event Trigger (EIS bright point trigger) status	Bits 6 to 7: Status value 1 = Enabled 2 = Disabled
12 & 13	TC_FAILED_PKTC	TC packets failed counter. This is a 16-bit	0 to (2^16 –1)

Byte No.	Name	Description	Range
		counter. This counter is initialised to 0 upon the ICU starting up and incremented by 1 for each TC packet failed to execute. This counter excludes status and memory dump requests. The likely cause of the command rejection is reported in byte 1 (TC_FAILED_EC). CMD BC1 = 0x23 is required to resets the counter to 0.	
14	TC_FAILED_CMD_ ID	The Command ID of the last packet failed. This is an 8-bit parameter. CMD BC1 = 0x23 is required to resets the counter to 0.	0 to (2^8 –1)
15	CMD_BUF_STAT	This parameter indicates the status of the command packets software buffer. The buffered commands exclude status and memory dump MDP requests. This buffer can hold up to 16 TC packets. A value of 0 indicates that the buffer is empty.	0 to (2^8 –1) NOTE: If the FIFO status becomes 12 (decimal), then the commanding needs to be slowed down (the ICU is falling behind). This may be caused by high latency commands (E.g. MHC Coarse mirror command)
16	XRT_FF_STAT	This parameter (2 bit) indicates the status of XRT flare flag (can be disabled internally by the ICU – Sequence command)	Bit 0,1: Status value 1 = Enabled 2 = Disabled
16	EIS_FF_STAT	This parameter (2 bit) indicates the status of EIS flare flag (can be disabled internally by the ICU – Sequence command)	Bit 2,3: Status value 1 = Enabled 2 = Disabled
16	HM_MON_STAT	This parameter (2 bit) indicates the status of the ICU health monitor (can be enabled or disabled by a ground command)	Bit 4,5: Status value 1 = Enabled 2 = Disabled
16	AEC_STAT	This parameter (2 bit) indicates the status of EIS AEC (can be disabled internally by the ICU – Sequence command)	Bit 6,7: Status values 1 = Enabled 2 = Disabled
17	MEM_DMP_ STAT	This parameter (2-bits) indicates the status of memory dump. Aborted flag is reported if there is a communication problem between the MHC or the CAM and the ICU. Under this condition the memory dump data cannot be acquired.	Bit 0,1: Memory dump values 1 = Running 2 = Idle 3 = Aborted
17	SEQ_STAT	This is a 3-bit parameter indicating the status of the current sequence.	Bit 2,3 and 4: Sequence status values 1 = Running 2 = Stopped 3 = Aborted 4 = Paused
17	MODE_EN_STAT	This is a 2 bit parameter indicating whether the mode transition is enabled via a ground command or not (CMD-ID 0x20). Also note this parameter is automatically disabled by the ICU when a trigger response (flare or event) is active to ensure that the flare response is not aborted accidentally by the OP/OG commands. The flag is re-enabled by the ICU after the response sequence has been	Bit 5,6: Mode transition enable status 1 = Enabled 2 = disables

Byte No.	Name	Description	Range
		completed. In order to manually abort the response sequence from the ground, re-enable made transition (Command BC1 0x20) and go back to Manual mode. Also the mode transition can be re-disabled using CMD BC1 0x22. Default: Disabled on ICU operational code start-up	
17	XRT_FF_REC	This is a 1-bit parameter indicating the last received flag from XRT via MDP. This field is copied from the MDP status request parameters.	Bit 7: XRT Flare Flag Status 0 = No Flare 1 = Flare
18	XRT_X_COR	This is an 8-bit parameter indicates the X-Coordinate as received from XRT via MDP. This field is copied from the MDP status request parameters.	Bit 0 to 7: Flare X-coordinate Range 0 to (2^8 – 1)
19	XRT_Y_COR	This is an 8-bit parameter indicating the Y-Coordinate as received from XRT via MDP. This field is copied from the MDP status request parameters	Bit 0 to 7: Flare Y-coordinate Range 0 to (2^8 – 1)
20	SEQ_I	This is an 8-bit parameter indicating the index of the sequence currently running or last run (if no sequence is running). The total number of EIS sequences is 128.	Bits 0 to 7: Sequence Index Range 0 to 127.
21	SEQ_P	This is an 8-bit parameter indicating the last sequence pointer position. Note that each sequence is 128 bytes long.	Bit 0 to 7: Sequence pointer value Range 0 to 127
22	LL_I	This is an 8-bit parameter indicating the line list Index currently in use or last used. The latter case if the sequence is no longer running	Bit 0 to 7: Line List Index Range 0 to 47
23	MD_BUF_STAT	This parameter indicates the status of the Mission Data software buffer. This buffer is capable of holding up to 5 Mission Data sub-packets. A sub-packet is 4 Kbytes long.	Bit 0 to 7: No. Of MD sub-packets in MD buffer Range 0 to 5.
24 & 25	EXPOSURE_NO	This parameter is a 16-bit counter indicating the exposure number, per raster. This parameter is initialised to 0 when starting a Raster and incremented by 1 for each raster exposure performed.	Bit 0 to 15: Exposure counter Range 0 to 0xFFFF
26 & 27	FINE_M_POS	This is a 16-bit parameter indicating the last commanded MHC Fine Mirror position. This parameter is acquired from the MHC when the shutter is closed, i.e. exposure information [4]. ***Note: Invalid means** 1 – Zero exposure time (shutter not used) 2 – Flat field, STIM or Test pattern CAM exposures (shutter not used) 3 – Communication problem between the ICU and the MHC (shutter used but not possible to acquire the MHC exposure information). For example RS422 link problem.	Bit 0 to 15: Fine mirror position Range 0 to (2^16 –1) Bit 0: mode 0 = Manual Mode 1 = Auto mode (sequence use) Bits 1 – 3: unused Bits 4 to 15: Fine mirror set point Range: 600 to 3000, which corresponds to 0-2400 mirror steps. 0xFFFF = Invalid *** See note**
28	ICU_VF	This is a 2-bit parameter indicating the current ICU status acquisition.	Bit 0 to 1: ICU status validation flag

Byte No.	Name	Description	Range
			Flag = 1 (valid) Flag = 2 (invalid)
28	PSU_VF	This is a 2-bit parameter indicating the current PSU Status validation flag. Invalid flag indicates a failure in the handshake between the ICU and PSU. The Handshake is performed via a validation bit in the acquired status parameters.	Bit 2 to 3: PSU status validation flag Flag = 1 (valid) Flag = 2 (invalid)
28	CAM_VF	This is a 2-bit parameter indicating the current CAM Status validation flag. Invalid flag indicates either the CAM is OFF [3] or a failure in the handshake between the ICU and CAM, when switched ON. The handshake is performed via a timeout for the status parameter acquisition. **Note that this flag will be INVALID following a CAM power ON or reset as the CAM enter Auto data generation mode. An EXIT_DEFAULT command is needed to validate this flag.**	Bit 4 to 5: CAM status validation flag Flag = 1 (valid) Flag = 2 (invalid)
28	MHC_VF	This is a 2-bit parameter indicating the last CAM Status validation flag. Invalid flag indicates either the MHC is OFF [3] or a failure in the handshake between the ICU and MHC, when switched ON. The handshake is performed via a timeout for the status parameter acquisition. **Note that the MHC validation flag may become INVALID when a lengthy MHC command is executed (e.g. Slit/Slot or CMIR move), as the MHC interface is locked for the command execution duration.**	Bit 6 to 7: MHC status validation flag Flag = 1 (valid) Flag = 2 (invalid)
29	ICU_ERROR_F	These flags are set to 0 when no errors are detected otherwise set to 1. Command error means that an error is encountered in the command interface The error cause is reported in byte 10 (internal error). A status error means that the status/memory dump hardware FIFO has not been emptied (via the ICU state machine) while a new packet becomes available. A MD error means that the ICU state machine has not transmitted the previous MD sub-packet when it requested a new one (noise problem). ICU, CAM, MHC status request error are ICU software processing anomaly indicating that the MDP issued a new status request while the previous status packet was not processed (acquired or sent) by the ICU. Similarly for the Memory Dump request error.	Bit 0 to 7: Error flags Bit 0: Command error Bit 1: Status error Bit 2: MD error Bit 3: ICU status request error Bit 4: CAM status request error Bit 5: MHC status request error Bit 6: Mem. Dump request error Bit 7: Task Manager/mode controller time-out error.

Byte No.	Name	Description	Range
		Task manager/mode controller time-out error means that a command is intended for a task while the task is not ready. For example, if a memory dump is requested while the previous request is still in progress, then this error flag is set. Note that when this error flag is set, the offending CMD-ID is logged in byte 14 to alert users about the problem. This error will most likely set if a task is engaged in lengthy operation (e.g. move course mirror or large memory dump) while a new ground command is sent to the task.	
30	XRT_ERROR	These error flags (warnings) are set in response to XRT flare response Bit 0 indicates an error is detected in the XRT control parameter table (CAM addresses or the response raster ID are set to 0 or all Fs, i.e. initialised OBS table values) Illegal values. Bit 1 indicates that either the response sequence is out of range or the sequence checksum has failed. Bit 2 is as in bit 1, but for the line list. Bit 3 indicates that the raster (as specified by the raster ID) could not be located in the response sequence. Bit 4 indicates that the EIS is in an incorrect mode to respond to XRT flare (not in Manual or Auto modes). Bits 5 and 6 indicate a communication problem between the XRT flare handling software task and the sequence interpreter or CAM handling tasks. Bit 7 is a flag (**warning**) indicates that XRT flare is outside EIS FOV. This flag will auto- reset if the next flare is within EIS FOV. CMD BC1 = 0x23 is required to resets these flags to 0.	Bit 0 to 7: Error flags / warnings Bit 0: Parameter error Bit 1: Response sequence error Bit2: Line list error Bit3: Raster error Bit4: Mode error Bit5: XRT task to sequence interpreter time-out Bit6: XRT task to CAM time-out Bit7: XRT flare coordinates outside EIS FOV warning
31	ASRC_STAT	Anti Solar Rotation Compensation status	Bits 0 to 1: Status value 1 = Enabled 2 = Disabled
31	MHC_LOAD_STAT	This parameter is updated in response to command BC1 0x2C. It indicates the status of MHC code transfer from the ICU EEPROM to the MHC RAM. Note that in normal operation, this flag should change from load in progress to stopped (~ 2 minutes). However, code loading aborted flag is set if the loading task	Bits 2 and 3: MHC code load status values are as follows: 1 = Load in progress 2 = Idle (stopped) 3 = Aborted

Byte No.	Name	Description	Range
		(memory manager) has a communication time-out with the MHC task (10 seconds time-out). Also abort status will be reported if the ICU failed to enable the EEPROM in order to acquire the MHC code. This latter will be reported in TC_FAILED_EC parameter.	
31	HC_STAT	Bake-out Heater controller [13] status. This parameter defaults to "stopped" on the ICU reboot and also following a bake-out operation completion when the heater duty cycle is reduced to 0. Idle state is entered following a bake-out mode change (30 seconds pause) to allow the ground to disable one of the CCDs heater relays in the unlikely event of a hardware fault. Aborted is entered if the heater duty cycle is commanded to a value grater than 100% or a bake-out mode change command is received (standby or emergency) while the heaters duty cycle is not 0. Normal mode change (standby) should be undertaken when the heaters duty cycle is reduced to 0 [13].	Bits 4 and 5: Bake out heater controller status 0 = Idle 1 = Running 2 = Stopped 3 = Aborted
31	HC_DUTY_ERROR	Heaters duty cycle error flag is set if heaters duty cycles command (power) update is received in less than 5 minutes (minimum update time is 5 minutes [13]). Note that the 5 minutes is the elapsed time between two commands reception. CMD BC1 = 0x23 is required to resets this flag to 0.	Bit 6: Heater controller duty cycle update error
31	HC_PSU_TO	Bits 7 error flag indicates a communication problem between the bake out heater software task and the PSU software task has occurred (5 seconds time-out). CMD BC1 = 0x23 is required to resets this flag to 0.	Bit 7: HC to PSU communication time out
32 & 33	PORT_READ	This parameter returns a port read value, in response to CMD-ID 0x27 [7].	Bits 0 to 15: Range 0 to 65535
34 & 35	MDP_LL_ERROR	MDP data line list error. This error is set if any MDP packet X or Y partial are not a multiple of 8. The offending **raster ID** is logged in this parameter to alert the user. This error will result in **aborting** the running sequence. CMD BC1 = 0x23 is required to resets this parameter to 0.	Range 0 to 65535
36 & 37	MHC_CMD_H	Rejected MHC Command Header. This parameter act as an advance warning that an MHC command was rejected (MHC NACK). The command rejection error code is reported in the MHC status (status type 3).	Bits 0 to 15: Last MHC Command header rejected [7] Range 0 to (2 ^ 16 –1). The MHC command headers are defined in [7].

Byte No.	Name	Description	Range
		CMD BC1 = 0x23 is required to resets this parameter to 0.	
38	EEPROM_STAT_1	EEPROM status following the EEPROM reset de-asserted (prior to read/write operations), i.e. not reset state. See appendix 1.	Bits 0 to 3: EEPROM status before access
38	EEPROM_STAT_2	EEPROM status following the EEPROM reset asserted (following read/write operations), i.e. reset state. See appendix 1.	Bits 4 to 7: EEPROM status after access
39	FT_ERROR	These error flags (warnings) are set in response to EIS flare trigger **response** Bit 0 indicates an error is detected in the FT control parameter table (CAM addresses or the response raster ID are set to 0), i.e. illegal values. Verify that EIS FT control parameters are loaded. Bit 1 indicates that either the response sequence is out of range or the sequence checksum has failed. Bit 2 is as in bit 1, but for the line list. Bit 3 indicates that the raster (as specified by the raster ID) could not be located in the response sequence. Bits 4 and 5 indicate a communication problem between EIS flare trigger handling software task and the sequence interpreter or CAM handling tasks. Bit 6 indicates that no line is marked for EIS flare trigger processing (line list error) CMD BC1 = 0x23 is required to resets these flags to 0.	Bit 0 to 7: Error flags Bit 0: Parameter error Bit 1: Response sequence error Bit2: Line list error Bit3: Raster error Bit4: FT task to sequence interpreter time-out Bit5: FT task to CAM time-out Bit 6: Window error Bit 7: spare bit
40	PSU_MARK	PSU HK table marker bit.	Bit 0: range 0 to 1. 1 = Valid, 0 = Invalid
40	PSU_SS_PRES_STAT	Sun sensor presence (unused)	Bit 1: range 0 to 1.
40	PSU_CCDB_BHTR_EN_STAT	CCD B bake-out heater status	Bit 2: range 0 to 1. 1 = Enabled
40	PSU_CCDA_BHTR_EN_STAT	CCD A bake-out heater status	Bit 3: ranger 0 to 1. 1 = Enabled
40	PSU_CCD_B_BHTR_ON_STAT	CCD B bake-out heater ON/OFF	Bit 4: range 0 to 1. 1 = ON
40	PSU_CCD_A_BHTR_ON_STAT	CCD A bake-out heater ON/OFF	Bit 5: range 0 to 1. 1 = ON
40	PSU_MHC_HTR_P28V_STAT	MHC operational heater +28V supply status	Bit 6: range 0 to 1. 1 = ON
40	PSU_MHC_MECH_P28V_STAT	MHC mechanism +28V supply status	Bit 7: range 0 to 1. 1 = ON
41	PSU_MHC_ELEC_P28V_STAT	MHC electronics +28V supply status	Bit 0: range 0 to 1. 1 = ON
41	PSU_MHC_MHTR_	MHC make-up heater status	Bit 1: range 0 to 1.

Byte No.	Name	Description	Range
	STAT		1 = ON
41	PSU_CAM_MHTR_ STAT	CAM make-up heater status	Bit 2: range 0 to 1. 1 = ON
41	PSU_CAM_P39V_ STAT	CAM +39V supply status	Bit 3: range 0 to 1. 1 = ON
41	PSU_CAM_N8V_ STAT	CAM –8V supply status	Bit 4: range 0 to 1. 1 = ON
41	PSU_CAM_P7V_ STAT	CAM +7V supply status	Bit 5: range 0 to 1. 1 = ON
41	PSU_CAM_P8V_ STAT	CAM +8V supply status	Bit 6: range 0 to 1. 1 = ON
41	PSU_CAM_P13V_ STAT	CAM +13V supply status	Bit 7: range 0 to 1. 1 = ON
42	PSU_CCD_A_TEMP	CCD A temperature	Range 0 to 255
43	PSU_CCD_B_TEMP	CCD B temperature	Range 0 to 255
44	PSU_PROC_TEMP	ICU processor temperature	Range 0 to 255
45		Unused	
46	PSU_ICU_P2.5V	ICU +2.5V supply	Range 0 to 255
47	PSU_ICU_P5V	ICU +5V supply	Range 0 to 255
48	PSU_ICU_P15V	ICU +15V supply	Range 0 to 255
49	PSU_ICU_N15V	ICU –15V supply	Range 0 to 255
50	PSU_ICU_P2.5I	ICU +2.5V supply current	Range 0 to 255
51	PSU_ICU_P5I	ICU +5V supply current	Range 0 to 255
52	PSU_ICU_P15I	ICU +15V supply current	Range 0 to 255
53	PSU_ICU_N15I	ICU –15V supply current	Range 0 to 255
54	PSU_MBUS_28V	Main bus 28V supply	Range 0 to 255
55	PSU_MBUS_28I	Main bus 28V supply current	Range 0 to 255
56	EEPROM_COPY_ R_STAT	EEPROM internal copy request. These parameters are set in response to EEPROM_COPY_ REQUEST command (BC1 = 0x2D). Initialised to **Invalid** on ICU operational code start-up.	Bits 0 to 3: **Source** EEPROM Range: 0 to 7 Bits 4 to 7: **Destination** EEPROM Range: 0 to 7 **0xFF**: **Invalid** request.
57	EEPROM_COPY_ P_STAT	EEPROM Copy status These statuses are reported in response to EEPROM COPY PERFORM command (BC1 = 0x2E). Aborted status is reported if either the EEPROM reset remove operation failed (hardware error) or a page is programmed incorrectly (write/read mismatch). These error conditions can be verified from EEPROM enable error or EEPROM programming error in TC_FAILED_EC parameter (byte #1).	Status: Bits 0 and 1 01b: Running 10b: Stopped 11b: Aborted
57	AEC_WIN_ERROR	AEC window marker not present in line list when AEC is run. If this error is set, then the AEC will run at ~22 seconds fixed exposure time (default AEC timetable middle position) [15]. CMD BC1 = 0x23 is required to resets this flag to 0.	Bit 2: Error flag 0 = No error 1 = Error
57	AEC_PARMS_	This flag is set if an error is detected in AEC	Bit 3: Error flag

Byte No.	Name	Description	Range
	ERROR	control parameter table (High and low energy pixel counts are either 0's or all 0xF's). If this error is set, then the AEC will run at ~22 seconds fixed exposure time (default AEC timetable middle position) [15]. CMD BC1 = 0x23 is required to resets this flag to 0.	0 = No error 1 = Error
57	AEC_TIME_ERROR	This error flag is set if an error is detected in the AEC timetable (delta time between the first 20 timetable entries = 0). If this error is set, then the AEC will run at ~22 seconds fixed exposure time (default AEC time table middle position) [15]. CMD BC1 = 0x23 is required to resets this flag to 0.	Bit 4: Error flag 0 = No error 1 = Error
57	Spare		Bits 5 to 7
58-59	Spare		
60 to 61	HM_OOL_ALERT	Health Monitor alert. Parameter out of limit value [14].	Range 0 to (2^16) - 1
62 to 63	HM_PSU_TO	PSU status to health monitor time-out	Bit 0: range 0 to 1 1 = Time-out error
62 to 63	HM_CAM_TO	CAM status to health monitor time-out	Bit 1: range 0 to 1 1 = Time-out error
62 to 63	HM_MHC_TO	MHC status to health monitor time-out	Bit 2: range 0 to 1 1 = Time-out error
62 to 63	HM_PSU_OOL	PSU OOL error flag	Bit 3: range 0 to 1 1 = PSU error
62 to 63	HM_CAM_OOL	CAM OOL error flag	Bit 4: range 0 to 1 1 = CAM error
62 to 63	HM_MHC_OOL	MHC OOL error flag	Bit 5: range 0 to 1 1 = MHC error
62 to 63	HM_PARM_ID	Sub-system OOL parameter identifier [14].	Bits 6 to 12: range 0 to 74
62 to 63		Spare bit	Bits 13
62 to 63	CAM_MHC_ POWER_ON	MHC and CAM turn ON via direct PSU power lines switching. These two flags have a value of 0 if the MHC and CAM are turned ON via EIS mode change (MAN mode). The primary purpose of these flags is to distinguish between EIS modes or direct PSU commanding sub-system turn ON's.	Bits 14 and 15 Bit14 = 1 (CAM ON via PSU) Bit15 = 1 (MHC ON via PSU)
64	LAST_BC1_R	Last command ID received	Bit 0 to 7: BC1 Range 0 to (2^8-1)
65	LAST_BC2_R	Last command BC2 received. Initialised to 0 if none.	Bit 0 to 7: BC2 Range 0 to (2^8-1)
66	LAST_BC3_R	Last command BC3 received. Initialised to 0 if none.	Bit 0 to 7: BC3 Range 0 to (2^8-1)
67	LAST_CMD_L_R	Last command received length. For example if a command consists of BC1 and BC2, then the length = 2.	Bit 0 to 7: Last command length Range: 1 to Max. Command size
68	CMD_IF_STAT_1	The ICU HW command interface status as found by the software (i.e. before used). See appendix 1.	NA
69	MD_IF_STAT_1	The ICU MD HW interface status as found by the software (i.e. before used). See appendix 1.	NA

Byte No.	Name	Description	Range
70	STAT_IF_STAT_1	The ICU HW Status interface status as found by the software (i.e. before used). See appendix 1.	NA
71	WD_IS_STAT_1	The ICU Watchdog status as found by the software following a re-boot. See appendix 1.	NA
72	CMD_IF_STAT_2	The ICU HW command interface status following the interface use by the ICU software. See appendix 1.	NA
73	MD_IF_STAT_2	The ICU HW MD-interface status following the interface use by the ICU software. See appendix 1.	NA
74	STAT_IF_STAT_2	The ICU HW Status interface status following the interface use by the ICU software. See appendix 1.	NA
75	WD_IF_STAT_2	The ICU Watchdog status following the interface use by the ICU software. See appendix 1.	NA
76 and 77	MHC_422_STAT	ICU-MHC interface (RS422) status register (as found by the ICU software (i.e. before used). See Appendix 1.	NA
78 to 79	CAM_IF_ERROR	Bit 0 indicates a failed attempt to send a command to the CAM. Bit 1 indicates a failed attempt to read data from ICU-CAM FIFO. Bit 2 indicates that the ICU-CAM FIFO was full when the CAM attempted to send more data (ICU processing error) BIT 3 indicates a corrupted frame acquired by the ICU (CAM error). Bit 4 indicates that the CAM FIFO was not empty while the ICU attempt to command the CAM. The FIFO should have been emptied by previous ICU call. Bits 5, 6 and 7 indicate that a CAM service request blocked by the CAM interface handler (CAM interface is busy). Bits 8, 9, and 10 indicate that no response was received from the CAM interface by the requesting task. Bit 11 indicates that the CAM has not generated an interrupt in response to CCDs read-out. Bit 12 indicates that the CAM has not generated an interrupt in response to CCDs flushing request. Bits 13 and 14 indicate the presence of communication problem between the ICU and CAM (noise problem or incorrect commanding).	Bit 0 to 15: Error flags Bit 0: ROE write error Bit 1: ROE FIFO read error Bit 2: ROE FIFO overflow Bit 3: HSL error detected Bit 4: ROE FIFO not empty error Bit 5: ROE HK request time-out Bit 6: ROE Sequence Interpreter request time-out Bit 7: ROE dump request time-out Bit 8: ROE HK time-out Bit 9: ROE Sequence Interpreter time-out Bit 10: ROE memory dump time-out Bit 11: ROE read-out sequence time-out Bit 12: ROE flush sequence time-out Bits 13 - 14: ROE response error 1 = ROE un-recognised command 2 = ICU un-recognised response 3 = ROE timed-out response Bit 15: Spare

Byte No.	Name	Description	Range
		CMD BC1 = 0x23 is required to resets these error bits to 0 (sets to 1 when an error is detected). Also EXIT_DEFAULT mode CAM command [7] will result in clearing these errors, as the start-up errors are not genuine.	
80 and 81	ROE_IF_STAT_1	ICU-CAM interface (RS422) status register This parameter specifies the status of the interface as found (before being accessed). See Appendix 1.	
82 and 83	ROE_IF_STAT_2	ICU-CAM interface (RS422) status register. This parameter specifies the status of the interface after being accessed.). See Appendix 1.	
84 to 85	HSL_IF_STAT_1	ICU-CAM High Speed Link status This parameter specifies the status of the interface as found (before being accessed). See Appendix 1.	
86 to 87	HSL_IF_STAT_2	ICU-CAM High Speed Link status This parameter specifies the status of the interface after being accessed.). See Appendix 1.	
88 to 89	MHC_422_STAT_2	ICU-MHC interface (RS422) status. This parameter specifies the status of the interface after being accessed by the software). See Appendix 1.	
90	SEQ_ABORT_ CODE	This is a 4 bit parameter specifies the reason why the sequence is aborted. Note: If a sequence is aborted due to Un-known sequence command error, then the sequence pointer position (reported in byte 21) should indicate the location of the offending command in the sequence. Line list error could mean one of two things: 1) Line list checksum error, if sets on its own 2) MDP data processing error, if set in conjunction with MDP_LL_ERROR parameter, bytes 34 and 35 (MDP pixel data is not in 8x8). Ground abort indicates that the sequence is either aborted via a ground command or spacecraft command, including MDP abnormal behaviour (no status requests for 10 seconds). Sequence interpreter to science time-out is set in the event of communication problem. Shutter failed indicates that the MHC shutter either: Cannot be opened (two consecutive attempts). There is no point in continuing the raster (dark exposures) Or: Attempting to close the shutter failed (two	Bits 0 to 3: Ground abort = 1 Sequence checksum error = 2 Un-known Sequence command = 3 Sequence out of range (recursive calls only) = 4 Zero exposures number specified in a raster = 5 Line List out of range = 6 Line list error = 7 Shutter failed = 8 Sequence interpreter to science time-out = 9 Sequence Repeat error = 10 Raster Repeat error = 11 Trigger abort (warning) = 12 Health Monitor abort = 13 MHC-CAM abort = 14 AEC abort = 15

Byte No.	Name	Description	Range
		consecutive close attempts and two consecutive find shutter index attempts). Sequence and raster repeat error means that a 0 number of repeats are specified. Sequence repeat range is from 1 to 255 and raster repeat range is from 1 to 4095. Trigger abort warning indicates that EIS flare; EIS event or XRT flare triggers have aborted the current sequence. This warning will reset to zero after the response sequence run is completed. Health Monitor abort indicates that the health monitor task aborted the sequence (OOL detected). MHC-CAM abort indicates that the sequence is aborted because of one of the following reasons: 1 - the MHC is no longer responding (MHC software crash or ICU-MHC communication link error, i.e. broken). 2 – CAM read-out problem, i.e. the CAM read-out sequence not running correctly (no CAM end of read-out interrupt). Note that the sequence is aborted if 3 consecutive read-out failed To identify the source, check CAM_IF_ERROR and MHC_IF_ERROR. AEC abort indicated that the AEC run time has lapsed. CMD BC1 = 0x23 is required to resets these error bits to 0.	
90 and 91	RASTER_RUN_ REM	This parameter is a 12-bit counter that indicates the number of raster run remaining. This counter is decremented when a raster is completed and the raster run(s) is completed when this counter reaches a value of 0. At this point the sequence goes to the next command following a raster loop back command.	Bits 4 to 15: Value (0 to 2^12-1)
92	SEQ_RUN_REM	This parameter is an 8-bit counter that indicates the number of sequence run remaining. This counter is decremented when a sequence is completed and the sequence run(s) is completed when this counter reaches a value of 0. At this point the running sequence is either terminate or call another sequence. The sequence run is completed when this counter reaches a value of 0.	Bits 0 to 7: Value (0 to 2^8-1)
93	CMD_ID_FAILED_ INT	This is an 8-bit parameter, which logs the last Command ID rejected internally by the ICU software. Note that the ICU generates	Bits 0 to 7: Value (0 to 2^8-1)

Byte No.	Name	Description	Range
		some commands internally (e.g. MHC safe command). Also this parameter logs the command IDs of failed MDP autonomously generated commands (BC1 = 1, 2, 3 and 4). The ICU rejects these commands if the number of command parameters is incorrect (ICU command interface problems). CMD BC1 = 0x23 is required to resets this parameter to 0.	
94 to 95	MHC_IF_ERROR	Bit 0 indicates that a checksum error is encountered in the MHC returned data (RS422 link noise problem). FIFO not empty indicates that not all the data is read from the previous access (residual data remained in FIFO). May well superseded by checksum error. Also glitches on the FIFO write line may result in this error. FIFO overflow indicates that data written to the ICU MHC FIFO while the FIFO was full, resulting in losing data. Bits 3,4 and 5 indicate a communication problem between the MHC handling task and other tasks. Bit 6 indicates that the MHC returned an incorrect header to the ICU. The MHC parameters consist of a header plus data. Bits 7,8 and 9 indicate a communication problem between a specific task and the MHC handling task. A time-out due to MHC software crash may result in any of these bits been set. Bit 10 indicates that the ICU failed to transmit data to the MHC (hardware error) Bit 11 indicate that the ICU has timed-out while waiting for the return of a byte (10 ms minimum per byte wait). Note that the time out is invoked while the MHC has returned at least one byte (MHC is alive) Bit 12 indicates that the MHC did not respond to an ICU command (150 seconds timeout). This may be caused by MHC software crash. Bit13 indicates that the MHC has not received any command from the ICU (140 seconds timeout). This indicates that the link between the ICU and the MHC maybe broken. Note that the MHC should receive at	Bit 0 to 13: Error flags Bit 0: Checksum error Bit 1: FIFO not empty error Bit 2: FIFO Overflow error Bit 3: MHC to HK time-out Bit 4: MHC to sequence interpreter time-out Bit 5: MHC to Memory manager time-out Bit 6: MHC incorrect header Bit 7: MHC HK request time-out Bit 8: MHC memory dump request time-out Bit 9: MHC sequence interpreter request time-out Bit 10: RS422 write error Bit 11: RS422 read error Bit 12: MHC not responding error Bit 13: MHC I am alive flag

Byte No.	Name	Description	Range
		least HK requests every 10 seconds, when powered. CMD BC1 = 0x23 is required to resets these error bits to 0 (sets to 1 when an error is detected).	
95	EEPROM_ERROR	EEPROM reset error indicates that following an EEPROM reset either the reset line remains not in reset state or the EEPROM access inhibit line remains 0 (inactive). When this flag is set in conjunction with byte 1, i.e. TC_FAILED_EC, then this indicates that this error is flagged in response to a ground command. However, if it is set on its own, then it indicates the error was generated in response to the ICU software attempted to place the EEPROM in reset state upon starting-up. EEPROM write error means that the EEPROM handling timing requirements are violated. Verify the content of EEPROM via memory dump and re-uplink errors portion(s). Note that this error is set in the EEPROM status register (see Appendix 1). This error condition is examined following each EEPROM reset assertion and de-assertion. Clearing the EEPROM status register error flag is handled by the ICU, internally. CMD BC1 = 0x23 is required to resets these error bits to 0 (sets to 1 by the ICU software when an error is detected).	Bit 14 and 15: range 0 to 2 2 = EEPROM reset error 1 = EEPROM write error
96	ET_ERROR	These error flags (warnings) are set in response to EIS event trigger operations. Bit 0 indicates an error is detected in the ET control parameter table (CAM addresses or the response raster ID are set to 0), i.e. illegal values. Verify that EIS ET control parameters table is loaded Bit 1 indicates that either the response sequence is out of range or the sequence checksum has failed. Bit 2 is as in bit 1, but for the line list. Bit 3 indicates that the raster (as specified by the raster ID) could not be located in the response sequence. Bits 4 and 5 indicate a communication problem between the ET handling software task and the sequence interpreter or CAM handling tasks. Bit 6 indicates that no line is marked for EIS	Bit 0 to 7: Error flags Bit 0: Parameter error Bit 1: Response sequence error Bit2: Line list error Bit3: Raster error Bit4: ET task to sequence interpreter time-out Bit5: ET task to CAM time-out Bit 6: Window error Bit 7: spare bit

Byte No.	Name	Description	Range
		event trigger processing (line list error) CMD BC1 = 0x23 is required to resets these flags to 0.	
97	HC_TARGET_T	Bake-out heater controller target temperature in PSU ADC unit. This value is updated if the control temperature is changed. It is also confirmed following bake-out mode invocation.	Bit 0 to 7: Control temperature Range: 0 to 255 (ADC unit)
98	HC_DUTY_CYCLE	Bake-out heater duty cycle. This value is updated at the start of each 20 seconds heater cycle.	Bit 0 to 7: Duty cycle Range: 0 to 100%
99	Spare		

2.2 The Camera status parameters:

The following section details the CAM status parameters [11], i.e. EIS status type 2.

Byte No.	Name	Description	Ranges
0	CAM_P5V1_DIG	+5.1V digital voltage	Bit 0 to 7: Voltage value Range: 0 to 255
1	CAM_P2V5_DIG	+2.5V digital voltage	Bit 0 to 7: Voltage value Range: 0 to 255
2	CAM_P5V_AN_A	+5V CCD-A analouge voltage	Bit 0 to 7: Voltage value Range: 0 to 255
3	CAM_P5V_AN_B	+5V CCD-B analogue voltage	Bit 0 to 7: Voltage value Range: 0 to 255
4	CAM_N5V_AN_A	-5V CCD-A analogue voltage	Bit 0 to 7: Voltage value Range: 0 to 255
5	CAM_N5V_AN_B	-5V CCD-B analogue voltage	Bit 0 to 7: Voltage value Range: 0 to 255
6	CAM_P36V_A	+36V CCD-A voltage	Bit 0 to 7: Voltage value Range: 0 to 255
7	CAM_P36V_B	+36V CCD-B voltage	Bit 0 to 7: Voltage value Range: 0 to 255
8	CAM_P12V_A	+12V CCD-A voltage	Bit 0 to 7: Voltage value Range: 0 to 255
9	CAM_P12V_B	+12V CCD-B voltage	Bit 0 to 7: Voltage value Range: 0 to 255
10	CAM_VOD_A	CCD-A VOD (real ADC value)	Bit 0 to 7: Voltage value Range: 0 to 255
11	CAM_VRD_A	CCD-A VRD (real ADC value)	Bit 0 to 7: Voltage value Range: 0 to 255
12	CAM_VSS_A	CCD-A VSS (real ADC value)	Bit 0 to 7: Voltage value Range: 0 to 255
13	CAM_VOD_B	CCD-B VOD (real ADC value)	Bit 0 to 7: Voltage value Range: 0 to 255
14	CAM_VRD_B	CCD-B VRD (real ADC value)	Bit 0 to 7: Voltage value Range: 0 to 255
15	CAM_VSS_B	CCD-B VSS (real ADC value)	Bit 0 to 7: Voltage value Range: 0 to 255
16	CAM_P5VI_DIG	+5V digital current	Bit 0 to 7: Current value Range: 0 to 255
17	CAM_P2V5I_DIG	+2.5V digital current	Bit 0 to 7: Current value Range: 0 to 255
18	CAM_P5VI_AN_A	+5V CCD-A analogue current	Bit 0 to 7: Current value Range: 0 to 255
19	CAM_P5VI_AN_B	+5V CCD-B analogue current	Bit 0 to 7: Current value Range: 0 to 255
20	CAM_N5VI_AN_A	-5V CCD-A analogue current	Bit 0 to 7: Current value Range: 0 to 255
21	CAM_N5VI_AN_B	-5V CCD-B analogue current	Bit 0 to 7: Current value Range: 0 to 255
22	CAM_P36VI_A	+36V CCD-A current	Bit 0 to 7: Current value Range: 0 to 255
23	CAM_P36VI_B	+36V CCD-B cuurent	Bit 0 to 7: Current value Range: 0 to 255
24	CAM_P12VI_A	+12V CCD-A curent	Bit 0 to 7: Current value Range: 0 to 255
25	CAM_P12VI_B	+12V CCD-B current	Bit 0 to 7: Current value

Byte No.	Name	Description	Ranges
			Range: 0 to 255
26	CAM_UP_T	CAM upper temperature	Bit 0 to 7: Temperature value Range: 0 to 255
27	CAM_LO_T	CAM lower temperature	Bit 0 to 7: Temperature value Range: 0 to 255
28	CAM_N10V_A	-10V CCD-A	Bit 0 to 7: Voltage value Range: 0 to 255
29	CAM_N10V_B	-10V CCD-B	Bit 0 to 7: Voltage value Range: 0 to 255
30		Spare monitor 1	Bit 0 to 7: value Range: 0 to 255
31		Spare monitor 2	Bit 0 to 7: value Range: 0 to 255
32	CAM_VOD	Bias register 1. Confirms CCDA and B VOD commanded values	Bits 0 – 3: CCDB VOD Bits 4 – 7: CCDA VOD
33	CAM_VRD	Bias register 2. Confirms CCDA and B VRD commanded values	Bits 0 – 3: CCDB VRD Bits 4 – 7: CCDA VRD
34	CAM_VSS	Bias register 3. Confirms CCDA and B VSS commanded values	Bits 0 – 3: CCDB VSS Bits 4 – 7: CCDA VSS
35	CAM_CONTROL_REG_1	Control register 1	Bit 0: Reserved Bit 1: Running 1 = Enable internal pattern generator 0 = Disable internal pattern generator Bit 2: Self test-n 0 = Use internal data pattern generator Bit 3: Stim isolate-n 0 = Isolate Stim generators Bit 4: CCDB VOG2 1 = Normal 0 = Low gain Bit 5: CCDA VOG2 1 = Normal 0 = Low gain Bits 6 – 7: Unused
36	CAM_CONTROL_REG_2	Control register 2	1 = Enabled Bits 0 – 3: Reserved Bit 4: CCDB L R/O chain status Bit 5: CCDB R R/O chain status Bit 6: CCDA L R/O chain status Bit 7: CCDA R R/O chain status
37	=	Reserved	
38	=	Reserved	
39	CAM_SEU_COUNTER	SEU counter. This counter is incremented either when an SEU is detected (error detection and correction is implemented), or attempting memory dump from the CAM RAM un-initialised area.	Bit 0 to 7: Count value Range: 0 to 255
The following are CAM PSU parameters, i.e. voltages and currents supplied by the PSU. These parameters are extracted from the PSU status and copied here.			
40	PSU_CAM_P39V	PSU +39V supplied	Bit 0 to 7: Voltage value Range: 0 to 255
41	PSU_CAM_P39VI	PSU +39V current supplied	Bit 0 to 7: Current value Range: 0 to 255
42	PSU_CAM_P7V	PSU +7V supplied	Bit 0 to 7: Voltage value Range: 0 to 255

Byte No.	Name	Description	Ranges
43	PSU_CAM_N8V	PSU –8V supplied to the CAM	Bit 0 to 7: Voltage value Range: 0 to 255
44	PSU_CAM_P8V	PSU +8V supplied	Bit 0 to 7: Voltage value Range: 0 to 255
45	PSU_CAM_P13V	PSU +13V supplied	Bit 0 to 7: Voltage value Range: 0 to 255
46	PSU_CAM_P7VI	PSU +7V current supplied	Bit 0 to 7: Current value Range: 0 to 255
47	PSU_CAM_N8VI	PSU –8V current supplies	Bit 0 to 7: Current value Range: 0 to 255
48	PSU_CAM_P8VI	PSU +8V current supplied	Bit 0 to 7: Current value Range: 0 to 255
49	PSU_CAM_P13VI	PSU +13V current supplied	Bit 0 to 7: Current value Range: 0 to 255
50	SPARE1		Bit 0 to 7: value Range: 0 to 255
51	SPARE2		Bit 0 to 7: value Range: 0 to 255
Additional ICU status parameters (slow changing parameters)			
52 to 55	CCD_BUF_ADD_F	CCD buffer address failed. This parameter is used in conjunction with the ICU status parameter (status type 1, byte 11) and logs the first address of the CCD buffer that failed. This parameter is initialised to 0xFFFFFFFF (invalid address) when the test starts and updated when an address read-write error is detected.	Range: 0 to 0xFFFFFFFF
56 to 59	CCD_BUF_COUNT	This parameter is used in conjunction with the previous parameter and logs the total number of read-write errors during CCD buffer testing. This parameter is set to 0 when the test starts and incremented by 1 for each error detected.	Range: 0 to 0xFFFFFFFF
60 to 63	MHC_ALIVE_SYSEC	This parameter is used in conjunction with MHC_IF_ERROR and logs the MHC system error code. The error code logged here in response to ICU-MHC communication failure.	See MHC status parameter #68 and #69
64 and 65	EIS_XRT_X	EIS translations of XRT flare position in the X-direction.	Bit 0: Sign value 0 = Positive 1 = Negative Bits 1 to 15: X position in arcseconds
66 to 67	EIS_XRT_Y	EIS translations of XRT flare position in the Y-direction	Bit 0: Sign value 0 = Positive 1 = Negative Bits 1 to 15: Y position in arcseconds
68 to 69	CMIR_POS_ARCS	Coarse mirror position in arcseconds. This value is translated from the MHC coarse mirror resolver reading (MHC status #48)	Bits 0 to 15: range 0 to 1780 arcseconds (TBC)
70 to 71	FMIR_OFFSET	Fine mirror set point offset setting.	Bit 0 to 15: range 0 to 65535 Default: 600
72 to 75	FMIR_SLOPE	Fine mirror slope setting.	Default: 122992
76 to 79	CMIR_SLOPE	Coarse mirror slope setting.	Default: 33020
80 to 81	CMIR_RES_PX	Coarse mirror + resolver limit (+X) setting	Default: 16691
82 to 83	CMIR_RES_NX	Coarse mirror - resolver limit (-X) setting	Default: 5228
84 to 85	MHC_RESPONSE_	MHC response time out setting in units of	Default: 150 seconds

Byte No.	Name	Description	Ranges
	TO	1 second. The ICU time-out if the MHC doesn't respond to a command for up to 150 seconds.	
86 to 87	FMIR_S_TIME	Fine mirror settling time setting, in units of ms, which defines the time required for the mirror to settle after moving it	Default: 700 ms
88 to 89	CMIR_SPAN_ARCS	EIS Coarse mirror span setting in arcseconds.	0 to 1780 (TBC)
90 to 91	EIS_XFOV	EIS FOV setting in arcseconds (FMIR scan range)	0 to 295
92 - 93	FT_XF	EIS flare trigger X location, pixel position within the flare detection line.	0xFFFF: No flair
94 - 95	FT_YF	EIS flare trigger Y location, pixel position within the flare detection line.	0xFFFF: No flair
96 - 99	FT_XBIN_PEAK	EIS flare trigger X-bin peak value. X bin is obtained by summing pixels in the X-direction (dispersion)	Range: 0 to 0xFFFFFFFF 0: No X-bin value above X threshold. Note that a value of 0xFFFFFFFF means invalid (initial value or FT is disabled).
100 - 103	FT_YBIN_PEAK	EIS flare trigger Y-bin peak value. Y bin is obtained by summing pixels in the Y-direction (spatial)	Range: 0 to 0xFFFFFFFF 0: No Y-bin value above Y-threshold. Note that a value of 0xFFFFFFFF means invalid (initial value or FT is disabled).
104 - 105	ET_XF	EIS event trigger X location, fine mirror raster position (steps).	0xFFFF: No event
106 - 107	ET_YF	EIS event trigger Y location, pixel position within the event detection line.	0xFFFF: No event
108 - 111	ET_XBIN_PEAK	EIS event trigger X-bin peak value. X bin is obtained by summing pixels in the X-direction (dispersion)	Range: 0 to 0xFFFFFFFF 0: No X-bin value above the X threshold. Note that a value of 0xFFFFFFFF means invalid (initial value or ET is disabled).
112 - 115	ET_YBIN_PEAK	EIS event trigger Y-bin peak value. Y bin is obtained by summing pixels in the Y-direction (spatial)	Range: 0 to 0xFFFFFFFF 0: No Y-bin above the Y-threshold. Note that a value of 0xFFFFFFFF means invalid (initial value or ET is disabled).
116-149	Spares		

2.3 The MHC status

This section defines the MHC status parameters [4]. Note that 150 bytes are allocated for the MHC and 150 bytes are defined. **Also note that all the MHC status parameters are 16-bit parameters**.

Note that in the following table, PARM # (1 to 75) appears in bytes 0 to 149 of the MHC status parameter (Status type 3), MS byte first.

PARM #	Name	Description	Range
1	MHC_SG_OP	PZT strain gauge output	Bit 0 and1: 00b Bit 2 – 15 Raw ADC output
2	MHC_P5VD	MHC +5V Digital voltage	Bit 0,1: 00b Bit 2 – 15 Raw ADC output
3	MHC_P15V_A	MHC +15V analogue voltage	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
4	MHC_N15V_A	MHC -15V analogue voltage	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
5	MHC_P15V_M	MHC +15V DC Motor voltage	Bit 0,1: 00b Bit 2 – 15 Raw ADC output
6	MHC_GRA_POS_AN	MHC Grating analogue position This is an analogue measurement of an optical encoder used to locate the grating calibrated optical focus position (nominal centre). It becomes valid and is updated only on a grating move command. It is non-zero at the centre position and valid for only a limited range around the centre position.	Bit 0 – 15 Raw step count
7	MHC_SS_POS_STEPS	MHC Slit/Slot motor position in motor step counts (step per bit)	Bit 0 – 15 Raw step count
8	MHC_P120V_PZT	MHC +120V PZT voltage	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
9	MHC_SGV_REF	Strain Gauge Source Voltage reference	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
10	MHC_P5V_D_I	MHC +5V Digital current	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
11	MHC_P15V_A_I	MHC +15V Analogue current	Bit 0,1: 00b Bit 2 – 15 Raw ADC output
12	MHC_N15V_A_I	MHC -15V Analogue current	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
13	MHC_CMIR_POS_STEPS	CMIR position in motor step counts (step per bit), relative to the boot-up position. This is a software tracking parameter. It is a signed number and is initialised to zero on power up or reset. The step count is incremented for forward movement and decremented for reverse.	Bit 0,1: 00b Bit 2 – 15 Raw step count
14	MHC_GND_I_REF	MHC current input ground reference	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
15	MHC_RDC_I	RDC current for latch-up monitoring	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
16	MHC_DB_T0	MHC Digital Board temperature. Group 0	Bit 0,1: 00b

PARM #	Name	Description	Range
		Thermistor 0.	Bit 2 – 15 Raw ADC output
17	MHC_BOX_T1	MHC box temperature. Group 0 Thermistor 1.	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
18	MHC_PB_T2	MHC Power Board Converter B switching FET TR6	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
19	MHC_PB_T3	MHC Power Board Converter A switching FET TR7	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
20	MHC_SLA_T4	SLA (SS) motor temperature. Group 0 Thermistor 4	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
21	MHC_SLA_T5	SLA (Shutter) motor temperature. Group 0 Thermistor 5	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
22	MHC_HARNSS_T6	MHC Harness. Group 0 Thermistor 6.	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
23	MHC_MIR_BASE_T7	Mirror assembly base. Group 0 Thermistor 7.	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
24	MHC_MIR_PZT_T8	Mirror assembly PZT. Group 0 Thermistor 8	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
25	MHC_MIR_MOTOR_T9	Mirror assembly motor. Group 0 Thermistor 9	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
26	MHC_GRA_MOTOR_T10	GRA assembly motor. Group 0 Thermistor 10	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
27	MHC_GRA_ASM_T1	GRA assembly. Group 0 Thermistor 11	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
28	MHC_PB_D4_T12	MHC Power Board +5VM rectifier D4. Group 0 Thermistor 12	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
29	MHC_REF_THER_0	Thermistor zero reference. Thermistor zero	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
30	MHC_CAL_THER_0	Thermistor calibration resistor 1000.00 ohms	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
31	MHC_HZ_T0	Heater Zone Temperature. Group 2 Thermistor 0 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
32	MHC_HZ_T1	Heater Zone Temperature. Group 2 Thermistor 1 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
33	MHC_HZ_T2	Heater Zone Temperature. Group 2 Thermistor 2 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
34	MHC_HZ_T3	Heater Zone Temperature. Group 2 Thermistor 3 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
35	MHC_HZ_T4	Heater Zone Temperature. Group 2 Thermistor 4 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
36	MHC_HZ_T5	Heater Zone Temperature. Group 2 Thermistor 5 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
37	MHC_HZ_T6	Heater Zone Temperature. Group 2 Thermistor 6 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
38	MHC_HZ_T7	Heater Zone Temperature. Group 2 Thermistor 7 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
39	MHC_HZ_T8	Heater Zone Temperature. Group 2 Thermistor 8 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
40	MHC_HZ_T9	Heater Zone Temperature. Group 2 Thermistor 9	Bit 0,1: 00b Bit 2 – 15: Raw ADC output

PARM #	Name	Description	Range
		Location: see [12]	
41	MHC_HZ_T10	Heater Zone Temperature. Group 2 Thermistor 10 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
42	MHC_HZ_T11	Heater Zone Temperature. Group 2 Thermistor 11 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
43	MHC_HZ_T12	Heater Zone Temperature. Group 2 Thermistor 12 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
44	MHC_HZ_T13	Heater Zone Temperature. Group 2 Thermistor 13 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
45	MHC_HZ_T14	Heater Zone Temperature. Group 2 Thermistor 14 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
46	MHC_HZ_T15	Heater Zone Temperature. Group 2 Thermistor 15 Location: see [12]	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
47	MHC_GND_F_REF	MHC zero reference. Final stage zero reference	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
48	MHC_CMIR_POS	RDC derived primary mirror position (resolver), 0.03302” per bit. Nominal Mirror centre position is 0xAAD0; FORWARD command moves mirror toward –X, and increases resolver output. Resolver output wraps from 0xFFFF to 0x0000. See [7] for details. Note that the ICU translates the resolver reading (CMIR position) to arcseconds, and report it in status type 2, bytes 68 and 69 (CMIR_POS_ARCS).	Bit 0 – Bit 15: Raw RDC output
49	MHC_SS_POS	RDC derived slit / slot position (resolver) 19.776 arc-sec / bit, or 324 steps per 90°. NOTE: Nominal slit/slot positions are defined by parameter table entries	Bit 0 – Bit 15: Raw RDC output
50	MHC_MOTOR_ OPT_ENC	Status of all optical encoders / enables. Only valid when a Motor is moved. Note that while the grating is moving, the MHC HK cannot be acquired, hence the change in the grating encoders is not accessible. Similarly, for the shutter, due to the fact that the shutter duration (open or close) is very short. However, the encoder’s states can be monitored using TEST_CMD_ENC (trouble shooting).	Bit 0 – 7: Not Used Bit 8: Grating encoder enable (1 = on, 0 = off) Bit 9: Grating encoder 1 Bit 10: Grating encoder 2 Bit 11: Grating encoder 3 Bit 12: Shutter encoder enable (1 = on, 0 = off) Bit 13: Shutter encoder 3 Bit 14: Shutter encoder 2 Bit 15: Shutter encoder 1
51	MHC_ACT_OPT_ ENC	Status of all actuator optical encoders / enables The status of the encoders should tell whether the clamshell doors are open or closed. Bit 0 indicates that the LED power is ON.	1 = TRUE 0 = FALSE Bit 0: Encoder LED powered ON Bit 1: Encoder HK updates Bit 2-7: spares Bit 8: Outer closed Bit 9: Outer open Bit 10-13: Spares Bit 14: Inner closed

PARM #	Name	Description	Range
		However, because of the short LED ON pulse time, this parameter may remain 0. However, bit 1, when set, indicates that the doors status is updated every MHC status packet. To enable the updates of this status parameter, PARM table #95 must be enabled first, confirmed via Bit 1 setting.	Bit 15: Inner open
52	MHC_GRA_SW_POS	Software tracked GRA position (i.e. steps from limit), 1 motor step per bit. This parameter is initialised to zero on reboot and incremented or decremented when the grating is moved (forward or reverse). Also sets to zero when reverse limit is reached.	16 bit signed step count
53	MHC_EXP_T1	Duration of last exposure (shutter open time) as calculated by MHC, MS WORD	32 Bit exposure time in 1 us ticks
54	MHC_EXP_T2	Duration of last exposure (shutter open time) as calculated by MHC, LS WORD	
55	MHC_PZT_DRIVE	High voltage output to PZT.	Bit 0,1: 00b Bit 2 – 15: Raw ADC output Range –10V to 120V (14 bit signed value)
56	MHC_ACT_STAT	State of each actuator, armed, disarmed and fire. ACT 1 = Rear (inner) door ACT 2 = unused ACT 3 = Front (outer) door ACT 4 = unused	ARMED = 1 POWER ON (fired) = 1 Bit 0: Act. 4 Backup arm state Bit 1: Act. 4 Prime Arm State Bit 2: Act. 3 Backup Arm state Bit 3: Act. 3 Prime Arm State Bit 4: Act. 2 Backup Arm state Bit 5: Act. 2 Prime Arm State Bit 6: Act. 1 Backup Arm state Bit 7: Act. 1 Prime Arm State Bit 8: Act. 4 Backup Power Bit 9: Act. 4 Prime Power Bit 10: Act. 3 Backup Power Bit 11: Act. 3 Prime Power Bit 12: Act. 2 Backup Power Bit 13: Act. 2 Prime Power Bit 14: Act. 1 Backup Power Bit 15: Act. 1 Prime Power
57	MHC_CAL_SRC_STAT	CAL LED source state.	ON = 1 OFF = 0 Bit 0 – 1: Spares Bit 2: Cal Source 2 State Bit 3: Cal Source 1 State Bit 4 - Bit 15: Spares
58	MHC_HTR_STAT	The state of the MHC heaters and QCMs when the MHC status request is sampled.	ON = 1 Bit 0: QCM 2 Heater State Bit 1: QCM 1 Heater State Bit 2: QCM 2 State

PARM #	Name	Description	Range
			Bit 3: QCM 1 State Bit 4: Heater 11 State Bit 5: Heater 10 State Bit 6: Heater 9 State Bit 7: Heater 8 State Bit 8: Heater 7 State Bit 9: Heater 6 State Bit 10: Heater 5 State Bit 11: Heater 4 State Bit 12: Heater 3 State Bit 13: Heater 2 State Bit 14: Heater 1 State Bit 15: Heater 0 State
59	MHC_QCM_MSW	Last enabled QCM integration count (32 bits) MSW	32 bit Elapsed time between N QCM clock cycles at 1 μsec per count. Where N is set by the QCM_COUNT_INTERVAL parameter
60	MHC_QCM_LSW	Last enabled QCM integration count (32 bits) LSW	
61	MHC_C_MON1_T	Contamination Monitor 1 temperature	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
62	MHC_C_MON2_T	Contamination Monitor 2 temperature	Bit 0,1: 00b Bit 2 – 15: Raw ADC output
63	MHC_QCM_INT_CLOCK	Last enabled QCM integration time, 1 QCM clock Cycle / Bit. Note that the QCM uses 1.6 KHz clock (0.625 ms per clock cycle). QCM integration time (ms) = clock count * 0.625.	16 bit clock count
64	MHC_CMD_REC	MHC command counter	16 bit count
65	MHC_CMD_ACK	Acknowledged command counter	16 bit count
66	MHC_CMD_NACK	Not acknowledged command counter	16 bit count
67	MHC_CMD_ID	Last MHC command ID received	16 bit MHC command ID
68	MHC_SEC_MSW	MHC S/W internal error code. Refers to the MHC software source list line number. Consult MHC engineer.	16 bit error code

PARM #	Name	Description	Range
69	MHC_SEC_LSW	MHC S/W internal error code. Aborted command is set if a command sent to the MHC while a mechanic is moving. Such a command could be either abort or safe MHC command. MHC internal error associated with MHC software detected error. Heater overload is associated with requesting more the two heaters ON at the same time (heater setting > 200%). Position limit reached means a mechanism move reached the range limit Run limit reached means the number of steps exceeded the allowed limit (as set in the MHC parameter table) Command time-out means that the MHC timed out while waiting for a command bytes transmit ion from the ICU (ICU-MHC communication problem) Command in progress means that the MHC received a second command while the current command execution is pending. Note the ICU controls command feeding to the MHC and such error may be due to communication error (e.g. noise) Checksum error means the MHC detected a command checksum error. Note that the ICU_MHC exchange data with internally generated checksum Invalid command means the MHC received unrecognisable command ID (hamming code) Function not enabled means an attempt to execute a command without enabling it first. For example attempt to move mechanism without sending enable motor command MHC buffer full means that the MHC input or output buffer is full Which indicates a software handshake failure between the ICU and the MHC. The rest of errors are self-explanatory. In order to reset these bits to 0, an MHC clear status error command, i.e. MHC CLEAR_ERROR command must be sent [7].	Bit 0: Aborted command Bit 1: MHC internal error Bit 2: Function time-out Bit 3: Heater overload request Bit 4: Position limit reached Bit 5: Run limit reached Bit 6: Invalid parameters number Bit 7: Invalid parameter value Bit 8: Motor over current Bit 9: Heater over current Bit 10: Command time out Bit 11: Command in progress Bit 12: Checksum error Bit 13: Invalid command Bit 14: Function not enable Bit 15: MHC buffer full
70	MHC_TIME_MSW	MSW elapsed time count since last reset in seconds	32 bit time since reset (1 ms per bit)
71	MHC_TIME_LSW	LSW elapsed time count since last reset in seconds	
72	MHC_SYS_STAT	MHC system status code. RAM code only. Bits 0, 1, 2 and 3 indicate how the MHC software was started. If Bit 5 is set (MHC entered AUTO safe), the cause (offending parameter) is reported	ACTIVE = 1 Bit 0: Watchdog enabled Bit 1: Watchdog event Bit 2: Power-up event Bit 3: Soft reset event Bit 4: RDC latch-up event

PARM #	Name	Description	Range
		in PARMS #74 and #75, Indexes 8 and 9. Memory mode: RAM = 0 ROM = 1 If bit 11 is set, then this is a definitive indication that the shutter was closed when the MHC was last powered down. However, if both bits 10 and 11 are not set, then the shutter status is un-known. Shutter synch flag indicates that find shutter index command was sent to the MHC (should be sent as part of the MHC initialisation). In order to clear the safe bit (exit safe mode), toggle AUTO safe command, "Disable" then "Enable" (CMD BC1 = 0x5F). Also resetting the MHC clear this bit.	Bit 5: System safe event Bit 6: Memory mode (RAM/ROM) Bit 7: Mechanism enable Bit 8: RDC Auto mode (nominal operation) Bit 9: RDC ON mode Bit 10: Shutter open flag Bit 11: Shutter Closed Flag Bit 12: Shutter Sync Flag Bit 13: FMIR Mode 0= Man 1 = Auto Bit 14: RAM checksum OK Bit 15: Auto MHC safe enabled
73	MHC_VAC_ GAUGE	Remote Vacuum gauge This parameter is invalid on re-boot and requires CMD BC1 (0X71) to obtain a valid reading.	Bits 0 and 1: unused (set to 0) Bit 2 – 15: Raw ADC output
74	MHC_PERFORM_ INDEX	This parameter refers to subcomutated parameters index. See table below.	Bit 0 to 15: Range 0 to 23
75	MHC_PERFORM_P ARM	This parameter refers to subcomutated parameters value. See table below.	Bit 0 to 15: Value

Parameters #74 and #75 definition is as follows:

PARM #74 (Index)	PARM #75	Range
0x0000	MHC Analogue board temperature	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0001	MHC Aux board temperature	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0002	MHC Voltage Reference	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0003	MHC Aux Board voltage reference	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0004	Cal 1 Led Current. This parameter is latched for a sub-commuting cycle, if the CAL ON time > 50 ms. The value is reset in the next sub-com cycle.	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0005	Cal 2 Led Current This parameter is latched for a sub-commuting cycle, if the CAL ON time > 50 ms. The value is reset in the next sub-com cycle.	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0006	Cal 1 Led Voltage This parameter is latched for a sub-commuting cycle, if the CAL	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output

PARM #74 (Index)	PARM #75	Range
	ON time > 50 ms. The value is reset in the next sub-com cycle.	
0x0007	Cal 2 Led Voltage This parameter is latched for a sub-commuting cycle, if the CAL ON time > 50 ms. The value is reset in the next sub-com cycle.	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0008	MHC Auto safe activation code MS-Word. Note that Auto safe in entered if the MHC detects an out of limit value.	Bit 0 - 6: Spare Bit 7: RS422 Dropout auto safe Bit 8: RAM Checksum auto safe Bit 9: Parameter Table Checksum auto safe Bit 10: -15V Current auto safe Bit 11: +15V Current auto safe Bit 12: +5V Current auto safe Bit 13: RDC Current auto safe Bit 14: +120V Voltage auto safe Bit 15: -5VA Voltage
0x0009	MHC Auto safe activation code LS-Word. . Note that Auto safe in entered if the MHC detects an out of limit value.	Bit 0: +5VA Voltage Safe Bit 1: -15V Voltage Safe Bit 2: +15V Voltage Safe Bit 3: +5V Voltage Safe Bit 4: +15VM Voltage Safe Bit 5: Power converter Over-temperature Safe A Bit 6: Power converter Over-temperature Safe Bit 7: MHC Over-temperature Safe Aux Board Bit 8: MHC v Safe Analogue Board Bit 9: MHC Over-temperature Safe Digital Board Bit 10: SS Over-temperature Safe Bit 11: GRA V Safe Bit 12: Shutter V Safe Bit 13: CMIR V Safe Bit 14: +PZT Over-temperature Safe Bit 15: RDC Current Safe
0x000A	MHC enabled heater list.	Enabled = 1 Bit 0 –3: Not used Bit 4: H11 Bit 5: H10 Bit 6: H9 Bit 7: H8 Bit 8: H7 Bit 9: H6 Bit 10: H5 Bit11: H4 Bit 12: H3 Bit 13: H2 Bit 14: H1 Bit 15: H0
0x000B	MHC –5V Analogue Voltage	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x000C	MHC +5V Analogue Voltage	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x000D	MHC Parameter table checksum	Bit 0 to 15: Range 0 to 65535
0x000E	MHC RAM checksum	Bit 0 to 15: Range 0 to 255
0x000F	S/W Version # chars 1 and 2	ASCII Coded
0x0010	S/W Version # chars 3 and 4	ASCII Coded
0x0011	S/W Trace Buffer Enables	Enabled = 1 Bit 0 – 13: Spare Bit 14: Motor trace enable (all Motors except shutter) Bit 15: Shutter trace enable
0x0012	+15V Motor Current RAM mode	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0013	RDC current from last motor move RAM mode	Bit 0 '0' Bit 1 '0' Bit 2 – 15 Raw ADC output
0x0014	RDC Tracking bits RAM mode	Bits 0 to 13: Spare (0) Bit 14: RDC B Bit 15: RDC A

PARM #74 (Index)	PARM #75	Range
0x0015	SPARE	0xAA55
0x0016	SPARE	0xAA55
0x0017	SPARE	0xAA55

Appendix: ICU Hardware interfaces statuses

These statuses are acquired from the PM ICU Backplane Definition [9] and included here for completion. Note that the symbol **(~) or (_n)** means active low signal.

Bytes 68 & 72 - CMD INTERFACE STATUS:

CMD_IF Status:

Bit No.	0	1	2	3	4	5	6	7
CMD_CTL	0	~BIT_ERR	~HF	~IRQ	~OVRFLOW	~EF	~FF	CMD_ENA

BIT_ERR(d46): when bit PMD46 is '0' it indicates a transmission error, i.e. the packet was not a multiple of 8-bit bytes.
HF(d45): 'FIFO half full Flag' – a logic '0' indicates the CMD_FIFO is half full (> 2 Kbytes).
IRQ(d44): the CMD_ENA signal defines the length of a packet. On the falling edge of this signal the packet will have been written to the CMD_FIFO and an interrupt is generated to the ICU. When an interrupt has been generated this is logic '0'.
OVRFLOW(d43): 'FIFO Overflow Error' - if the CMD_FIFO is full when a new byte is ready to be written an overflow condition is indicated on bit PMD43. Logic '0' indicates an overflow.
EF(d42): 'FIFO Empty Flag' – a logic '0' indicates the CMD_FIFO is empty. Bit PMD42 shows the current state of the ~EF flag of the CMD_FIFO.
FF(d41): 'FIFO Full Flag' - a logic '0' indicates the CMD_FIFO is full (4 Kbytes). Bit PMD41 shows the current state of the ~FF flag on the CMD_FIFO.
CMD_ENA(d40): when bit PMD40 is at logic '1' this signal indicates that the interface is active and that a packet is being transmitted.

Bytes 69 & 73 - MD INTERFACE STATUS:

MD_IF Status:

Bit No.	0	1	2	3	4	5	6	7
MD_CTL	0	~FF	~EF	BSY	~IRQ	~EOP	~GO	0

FF (d46): 'FIFO Full Flag' - bit PMD46 is set to logic '0' when the MD_FIFO is full (8 Kbytes).
EF (d45): 'FIFO Empty Flag' – bit PMD45 is set to logic '0' when MD_FIFO is empty.
BSY (d44): 'BUSY' – this is an MDP signal, which indicates that the MDP is still busy processing the last packet data.
IRQ (d43): an interrupt is generated when the final word of the packet has been transmitted as indicated by the falling edge of the MD_ENA signal. Bit PMD43 latches the state of the interrupt signal.
EOP (d42): 'End of Packet' – when this is set to '1' it indicates that there are further sub-packets to transmit. Logic '0' indicates that the sub-packet data loaded into the MD_FIFO is the last of the current packet data.
GO (d41): this is the current state of the ~GO bit. It initiates the start of the state machine, which controls the interface. Logic '0' at PMD41 indicates when data from the MD_FIFO is being transmitted.

Byte 70 & 74 - EIS STATUS INTERFACE STATUS:

ST_IF Status:

Bit No.	0	1	2	3	4	5	6	7
ST_CTL	~ST_GO	0	0	0	0	~EF	~FF	ST_ENA

ST_GO (d47): this is the current state of the ~GO bit. It initiates the start of the state machine, which controls the interface. A '0' value at PMD47 indicates when data from the ST_FIFO is being transmitted.
EF (d42): 'FIFO Empty Flag' – bit PMD42 is set to logic '0' when ST_FIFO is empty.
FF (d41): 'FIFO Full Flag' - bit PMD41 is set to logic '0' when the ST_FIFO is full.
ST_ENA (d40): when bit PMD40 is at logic '1' this signal indicates that the interface is active and that a packet is being transmitted.

Bytes 71 & 75 - WD and TI INTERFACE STATUS:

WD Status:

Bit No.	0	1	2	3	4	5
WD_CTL	~WD_TRIP	~WD_EN	WD_TOSEL	~V_Fail	~ICU_Res	0

WD_TRIP (d47): 'Watchdog Trip' status – when bit PMD47 is '0' it indicates that a watchdog trip has occurred. On power-ON this is set to '1'. **The TRUE value for this bit is available in byte 71 (WD initial status).**
WD_EN (d46): 'Watchdog Enable' status – a '0' in bit PMD46 indicates that the watchdog circuit is enabled. On power-ON this is set to '1', i.e. default to "**DISABLED**" by the ICU hardware. The watchdog can only be enabled by the ICU software.
WD_TOSEL (d45): 'Watchdog Time-Out Select' – with bit PMD45 set to '1' the time-out period is set to 40 seconds. With bit PMD45 set to '0' the time-out period is 80 seconds. On power-ON this is set to '1', i.e. 40 seconds time-out.

WD V_Fail(d44): ICU reset caused by voltage failed (active low)
ICU_Res(d43): 'ICU Reset' – a '0' indicates that the ICU is reset via a ground command.

Bytes (76-77) & (88-89) - MHC RS422 interface status

MHC_422_STAT: MHC RS-422 status structure

Bit no.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	X	X	X	FIFO NE INT E	FIFO NF INT E	FIFO F INT E	Xmit not busy INT E	INT E	X	X	X	FIFO LD	FIFO E	FIFO NF	FIFO F	Xmit busy

All status bits are active **(high)**, unless specified

FIFO NE INT E: FIFO not empty interrupt enabled
FIFO NF INT E: FIFO nearly full interrupt enabled
FIFO F INT E: FIFO full interrupt enabled
Xmit not busy INT E: RS-422 transmit not busy interrupt enabled

INT E: Enable interrupts (must be enabled to enable one or more of the above interrupts)
FIFO LD: FIFO lost data. MHC attempting to write data to FIFO while the FIFO is full
FIFO E: FIFO empty
FIFO NF: FIFO nearly full (24 bytes or more present in FIFO)
FIFO F: FIFO full (32 bytes present in FIFO)
Xmit busy: RS-422 Transmit line busy

Bytes (80-81) & (82-83) - CAM RS422 interface status:

ROE_422_STAT: ROE (CAM) RS-422 status structure

Bit no.	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	X	X	EOF INT E	FIFO NE INT E	FIFO NF INT E	FIFO F INT E	Xmit not busy INT E	INT E	X	X	EOF DET	FIFO LD	FIFO E	FIFO NF	FIFO F	Xmit busy

All status bits are active **(high)**, unless specified

EOF INT E: Enable EOF interrupt
FIFO NE INT E: FIFO not empty interrupt enabled
FIFO NF INT E: FIFO nearly full interrupt enabled
FIFO F INT E: FIFO full interrupt enabled
Xmit not busy INT E: RS-422 transmit not busy interrupt enabled
INT E: Enable interrupts. Global disable. Must be enabled to enable any of the interrupts above
FIFO LD: FIFO lost data. CAM attempting to write data to FIFO while the FIFO is full
FIFO E: FIFO empty
FIFO NF: FIFO nearly full (3 bytes or more present in FIFO)
FIFO F: FIFO full (4 bytes present in FIFO)
Xmit busy: RS-422 Transmit line busy

Byte (84-85) & (86-87) - ROE HSL interface status:

HSL_IF_STAT: ROE (CAM) High Speed Link (HSL) status

Bit no.	0	1	2	3	4	5	6	7	8 - 15
	X	P_11	P_10	P-01	P_00	CCD BANK	L_ERROR	EOF-D	Last received EOF byte

All status bits are active **(high)**, unless specified
P_11: Port 11 is selected (CCD-B left hand side)
P_10: Port 10 is selected (CCD-B right hand side)
P_01: Port 01 is selected (CCD-A left hand side)
P_00: Port 00 is selected (CCD-A right hand side)
CCD BANK: CCD bank selected (bank 0 or 1)
L_ERROR: Link Error Detected while transferring data over link (corrupted frame)
EOF-D: EOF detected, i.e. all CCD data are read-out and written to CCD buffer
Last received EOF byte: Last value written by HLS (should be 0xCC for correct operation)

Byte (38) – EEPROM status register:

Bit No.	0	1	2	3
	Reset_n	Access Inhibit	Write Error	Write In Progress_n

Reset_n: EEPROM reset state (0 = reset state).
Access Inhibit: EEPROM read/write status (1 = inhibit), i.e. no read or write is allowed.
Write Error: Active high (1) indicates that an EEPROM write error has occurred.
Write in Progrss_n: Active low (0), which indicates that transfers from the EEPROM internal 128-byte page buffer to the actual EEPROM page is taking place.