Solar B – EIS

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FM ICU Hardware Design Definition

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1 Introduction

This document defines the design of ~~processor and~~ the digital electronics for the flight model of the ICU, as specified in AD1.

2 Scope

Where requirements can not be fulfilled, or have to be de-rated due to constraints of present technology, power budgets, mass budgets, physical space requirements or cost, a reference shall be recorded.

The power supply unit (PSU) is described in AD7.

3 Applicable Documents

AD1:	MSSL/SLB-EIS/SP012	EIS ICU Design Requirements
AD3:	MSSL/SLB-EIS/SP003	SOLAR B - EIS ICD Document
AD4:	SLB-120	Solar-B Electrical Design Standard
AD5:	MSSL/SLB-EIS/DD001	Electrical Block Diagram
AD6:	MSSL/SLB-EIS/DD006	EIS ICU Software Architectural Design

4 ICU Digital Electronics

Below is the block diagram of the ICU digital electronics.

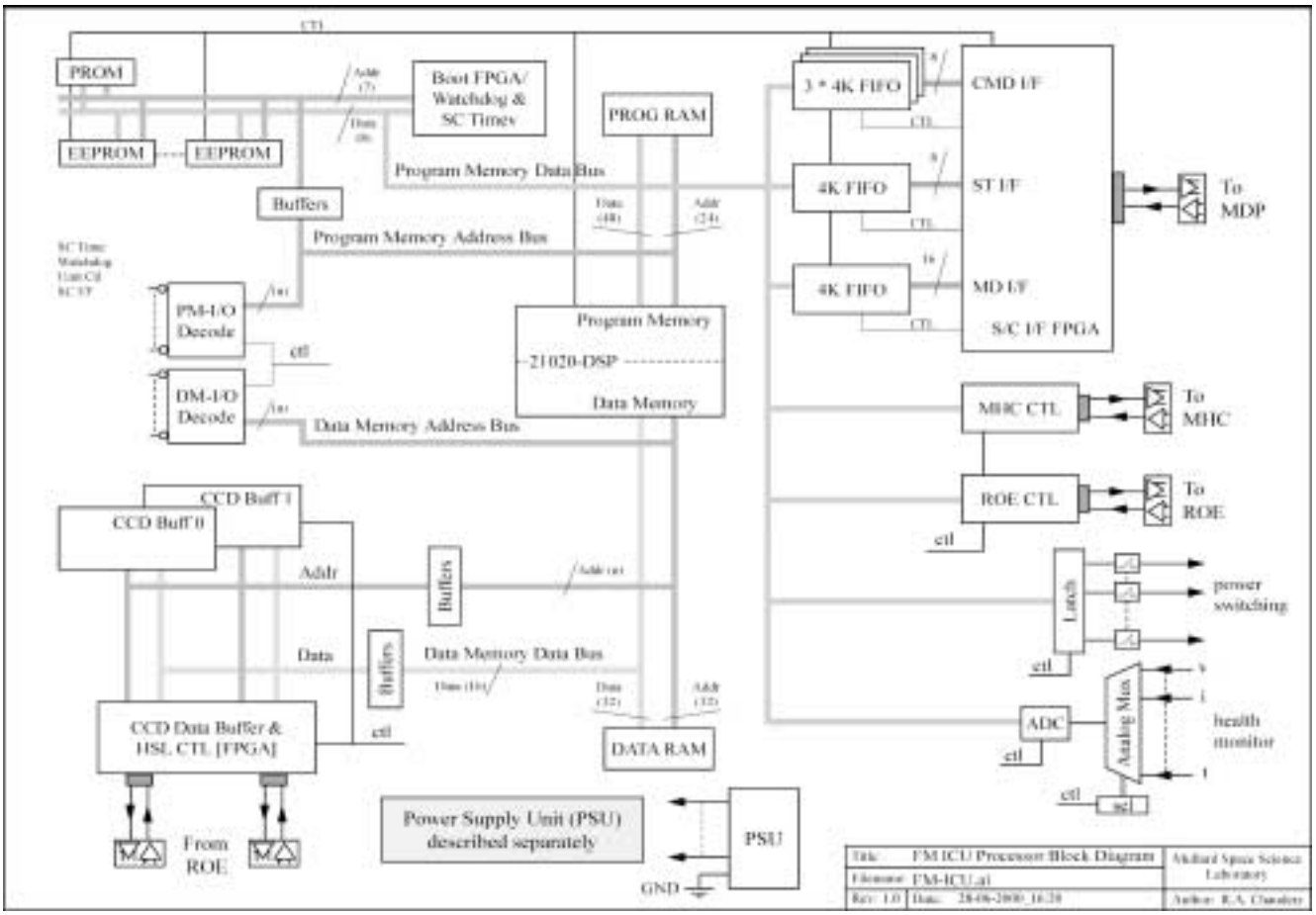

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Figure 4-1 Flight Model ICU Digital Electronics

The FM_ICU design is partitioned as four boards. These have the following functions:

Board #	Board	Board Function	Note
0	PSU	Primary power in	see AD7 for details
		Secondary power lines conditioning	
		Main power relay	
1	CM_CTL	Bus buffers & I/O decode	
		CCD buffers	2 * 2M by 16-bit SRAM
		CCD Buffer/High Speed Link (HSL) control FPGA	54SX16 Actel #3
		MHC/ROE control	2 * UART I.C.'s
		Working RAM	512k by 16-bit SRAM
2	SC_PROC	I/O Decode	
		Processor	21020 DSP running at 20MHz
		S/C interfaces FPGA	54SX16 Actel #1
		S/C interface FIFO's	4k by 9-bit FIFO
		S/C time FPGA	54SX16 Actel #2
		Watchdog FPGA	54SX16 Actel #2
		Volatile Program storage	6 * 128k by 8-bit SRAM
		Volatile Data storage	4 * 128k by 8-bit SRAM
		Permanent Code Storage	8/16k by 8-bit PROM
		Non-volatile Code storage	n * 128k by 8-bit EEPROM
3	MONITOR	Bus buffers & I/O decode	
		Heater switching & control	Bi-level switching
		ROE/MHC power line switching control	Bi-level switching
		Temp./voltage/current monitoring	Analogue I/P's

Table 4-1 FM ICU Boards

4.1 Space Craft Interface & Processor Card - (SC_PROC) – Board #2

4.1.1 21020 DSP

The SC_PROC board shall use a space qualified DSP manufactured by TEMIC or Lockheed Martin: the final choice of manufacturer will depend upon detailed specification of the individual device, and availability/price. The flight part DSP is packaged as a 256-pin MQFP.

The TEMIC TSC21020E processor is available from Matra MHS (France) to a radiation level of 50Krad, which has a SEL value of >100 Mev.mg/cm^2 and SEU rate of >50 Mev/mg/cm^2.

The architecture of the processor is based upon the Analog Devices ADSP-21020 DSP, and is fully compatible with it. The 21020 DSP has on-chip instruction cache, allowing each instruction to be executed in a single cycle. The off-chip Harvard architecture allows both the PROGRAM and DATA memory sides to process data simultaneously.

The 21020's JTAG port allows code from a host computer to be uploaded/downloaded to/from the DSP system; this also allows (virtually) real-time debugging of running software.

The EIS ICU shall be designed to run at 20 MHz.

4.1.2 Space Craft Interface FPGA – (SC_IF)

Command, status and mission data are transmitted and received over three serial interfaces in a packet structure. Full specifications are given in AD3. The interfaces, between the EIS ICU and the space craft (via MDP), are:

- COMMAND interface (CMD_IF) – base unit of packet is 8-bit
- STATUS interface (ST_IF) – base unit of packet is 8-bit
- MISSION DATA interface (MD_IF) – base unit of packet is 16-bit

The software communicates with the interfaces via status registers (STAT_REG) and data ports on the FIFO's. Three FIFO banks are connected to the SC_IF FPGA for temporary buffering of the incoming COMMAND, outgoing STATUS, and outgoing MISSION DATA packets.

All three interfaces are implemented in one 54RTSX16 Actel FPGA to the specification of AD3. Figure 4.3-1 shows the top-level symbol for the device connected to the data-packet FIFO's.

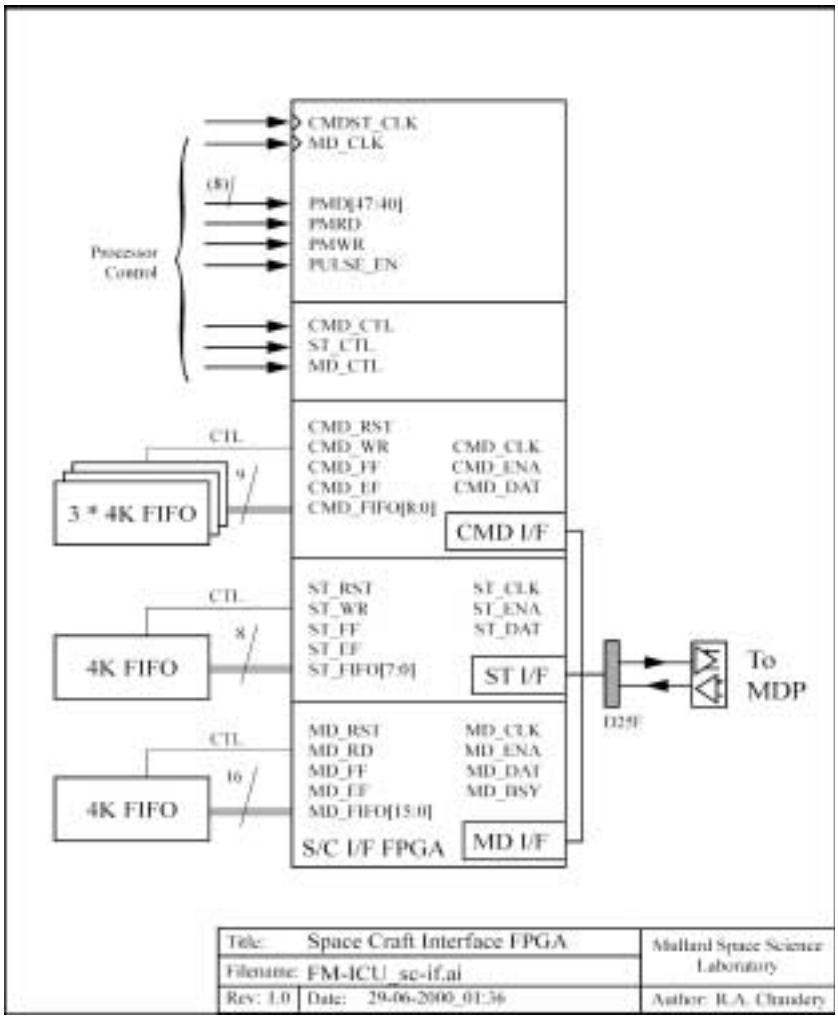

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Figure 4.3-1 Space Craft Interface FPGA (SC_IF)

Initially no data is transmitted to the MDP: the ICU will (nominally) wait for a command packet via CMD_IF and will only commence sending status data via ST_IF in direct response to a status or memory request command. Only after EIS has been commanded to begin an observation, image data is ready for transmission and the MDP is ready to receive mission data, will CCD image data be transmitted over the MD_IF.

A detailed description of the software control of these interfaces is given in AD6.

4.2 Space Craft Interface FIFO's

The MD interface has a sub-packet size of 4kbytes, so it has been decided to standardise on a FIFO of this minimum depth. The part being used is 4kbytes * 9-bit.

At present the only space qualified FIFO part that can be found has a relatively low SEU rate (~4-5 Mev/mg/cm^2).

This is not regarded as being too critical for the ST_IF circuit as the information transmitted over this interface is house keeping, EIS health monitoring information and down-linking of memory code space.

This is also not regarded as being too critical for the MD_IF circuit as information transmitted over this interface is CCD image data.

However, the FIFO forms a critical component of the CMD_IF circuit. Via this interface the EIS instrument receives all commanding, so it is vital that data is not corrupted. If no replacement part with a higher SEU rate is available then a method has to be found to increase the SEU figure for the present FIFO. There are three available options to achieve this aim:

Option	Method	Advantage	Disadvantage
1	add extra shielding to CMD_FIFO	Bread Board model does not need to be modified	mass budget increase
2	double –buffer using RAM	can use RAM device being used elsewhere with high SEU rate	increase in circuit complexity/parts and board space
3	implement triple-voting of FIFO data in software	easy to implement into design – no impact on SC_IF FPGA	increase in software complexity as it performs voting scheme

Table 4.4-1 FIFO SEU Trade-off

Option #1 is not viable because of extreme constraints on the mass budget.

Option #2 is not viable as it increases circuit complexity and board space whilst decreasing reliability owing to the increased number of parts being used.

Option #3 allows the existing SC_IF FPGA design to be used without any modifications. CMD_IF packet data (as 8-bit data) is received and?? written in parallel to three FIFO's. The FIFO data is then read out as 3 8-bit fields (24-bit words), which are then compared in software. In the nominal case all three bytes will be identical. When one of the bytes has had a SEU occur, a bit will have been flipped, causing only one of the three bytes to be different. The majority vote in software, in such a case, will decide the value of the byte in question when there is a conflict.

This method can only detect/correct for the case when only one of the three FIFO's has been upset by a SEU. It is very unlikely that multiple FIFO devices will suffer a simultaneous SEU at the same address, and so the effective CMD_FIFO SEU rate is increased to a point when it can be regarded as being immune. This is the system illustrated in figure 4.3-1 for the CMD_IF.

4.3 Command Interface Detailed Design – (CMD_IF)

TBD – [add state machine diagram, block diagram of circuit, design description] –

The operation of the CMD_IF is as in figure TBD, which shows the state machine for the control of the interface.

4.4 Status Interface Detailed Design – (ST_IF)

TBD – [add state machine diagram, block diagram of circuit, design description] –

The ST_IF FIFO uses a 4kbyte x 9-bit FIFO with only the lower 8-bits being used.

The operation of the ST_IF is as in figure TBD, which shows the state machine for the control of the interface.

The interface software module writes one complete packet as 8-bit bytes to the ST_FIFO. Once a full packet has been written to the ST_FIFO, the program issues a "GO" instruction to the ST_IF. This then initiates the start of the ST_IF state machine and automatic transmission of the data in the FIFO to the MDP.

As a status packet is only sent in response to a command, there is no need for additional hardware to generate interrupts or for software to poll the ST_IF STAT_REG.

4.5 Mission Data Interface Detailed Design – (MD_IF)

TBD – [add state machine diagram, block diagram of circuit, design description] –

The MD_IF FIFO is implemented as two 4kbyte x 9-bit FIFO's connected in width expansion mode to give a 4kbyte x 16-bit FIFO.

The operation of the MD_IF is as in figure TBD, which shows the state machine for the control of the interface.

The interface software module can write up to 4kbyte long sub-packets as 16-bit words to the MD_FIFO. Once a sub-packet has been written to the ST_FIFO, the program issues a "GO" instruction to the MD_IF. This then initiates the start of the MD_IF state machine and automatic transmission of the data in the FIFO to the MDP.

The MD_IF hardware will issue an interrupt to the processor when the mission data packet has been sent: the software may at that point load the next sub-packet and repeat the above process.

4.6 MDP-ICU Interface Differential Driver Circuits

The differential interface circuits between the MDP and ICU are as shown in ICD document AD3 sections 4.3 - 4.5. [add details of HS-26C31/32 devices here – *NOTE these are SMD devices* - design description]

4.7 Space Craft Time Function FPGA - (SC_Time)

[Describe this FPGA]

Space Craft time functions are designed in an Actel.

Watchdog functions are designed in an Actel.

128k * 48-bit RAD tolerant static RAM for program instructions storage with 35ns/45ns access speed giving zero wait state access.

128k * 32-bit RAD tolerant static RAM for data/variables storage with 35ns/45ns access speed giving zero wait state access.

512k * 16-bit RAD tolerant static RAM providing a secondary buffer area for data packets with 100ns access speed requiring 3 wait state.

4.8 Boot Function FPGA - (SC_Time)

the BOOT-FPGA provides a simple hardware solution to overcome the requirement of six-byte-wide instruction space for PROM. The FPGA holds the DSP in reset whilst the boot-code, stored as sequential bytes in PROM, are copied to six-byte-wide Program RAM (as required by the DSP).

*8/16k * 8-bit RAD tolerant PROM to hold the permanent BOOT-CODE.*

*128k * 8-bit * TBD devices of RAD tolerant EEPROM. The EEPROM, used as a byte-wide device, provides a default set of observing tables/sequences, and operational code. The data in EEPROM can be updated from and copied to Program/Data space RAM by the DSP.*

4.9 Camera-Mechanisms Control Card (CM_Ctl) new BOARD (“2)

The main functional blocks of this card are:

- two UART interfaces used to control the ROE and MHC. These have RS-422 specification line drivers.
- bus buffers for the processor address, data and control signals on and off the card.

An Actel is used to implement the high-speed interface from the camera electronics to the ICU. The same FPGA also controls the writing of image data to memory. The four CCD read-out ports are mapped to four blocks of CCD data buffer memory.

CCD image data buffers (CCD_BUF) are implemented as two pages: at any one time one page is available to the DSP for read/write operations, the other is available to the high-speed data links to stream CCD data to.

4.9.1 CCD Image Data Interface

This shall comprise two high speed data links from CAMERA to ICU running at 16MHz and shall use a three wire system to transmit data:

a) an enable signal which is active all the time whilst data is being transmitted.

b) a clock signal which is active whilst the enable signal is active.

c) serial data line. Data is transmitted on the falling edge of the clock signal.

The interface shall be is a unidirectional interface from CAMERA to ICU.

When the "enable" signal is deserted for more than TBD microseconds this shall infer to the ICU that all present exposure data has been sent.

The ICU will be in control of switching (alternating) the two CCD buffers.

4.9.1.1 CCD Image Data Format

To allow minimum cadence, the ICU has two CCD buffer areas on the ICU. These are alternately switched to connect to the CAMERA or ICU, thus data from the present exposure can be downloaded to one CCD buffer whilst the data from the previous exposure data is processed from the other CCD buffer.

Each CCD buffer will be able to hold two complete CCD images i.e. 2 * 2048 * 512 = 2M * 16 bit. There for total RAM requirements for the CCD buffer is 4Mwords (8Mbytes).

It will be a 16-bit word format with data being transmitted msb first.

The word is formatted as:

a) bit-14 and bit-15 will be used as ID bits to map to the CCD image area being read from.

b) 14-bit CCD data (bit-0 to bit-13)

The ID bits are used in the ICU to "auto-sort" CCD data to one of four pre-defined RAM address ranges.

5 ICU Parts Requirements

5.1 Memory Requirements

a) All memory (PROM, EEPROM, Program RAM, Data RAM) and interfaces (ports) will be uniquely mapped.

5.1.1 Boot PROM

- The "Boot-Loader" will be designed so that after RESET, it copies Boot-Code from 8 bit PROM to a 48-bit Program RAM area, whilst the rest of the ICU is held in a reset state.

5.1.2 EEPROM

- These will be mapped to two separate address ranges: the first bank will hold a working copy of operational code and a default Exposure-Set-up-Table; the second bank will hold code being patched from ground.
- All control of these operations will be under s/w control.
- EEPROM size will be 128k(TBD) * 48-bit(TBD)
- Exposure-Set-up-Tables will be kept in EEPROM.
- There is a WRITE operations life-cycle issue associated with EEPROM's so changes will need to be controlled (method TBD).

5.1.3 Program RAM

- RAM size will be 128k * 48-bit.

5.1.4 Data RAM

- CCD buffers will be in Data Ram address space.
- Working Area RAM will be 512k * 16-bit.

5.2 Watchdog

- This will be a 16 second period counter. Its terminal count pin will connect to the RESET circuit. If the counter is not reset within the 16 sec period then RESET circuit will be activated, causing a "WARM-REBOOT" to occur.
- There will be a h/w register for STATUS/Control of the Watchdog circuit:
- Counter reset bit (WRITE)
- WARM-REBOOT Flag (READ)
- Reset WARM-REBOOT Flag (WRITE)
- Enable/Disable Watchdog Flag (READ)
- Enable/Disable Watchdog circuit (WRITE)
- This register will not be routed to the global RESET signal, so that the status of the WARM-REBOOT flag is not lost after a watchdog trip occurs.

5.3 Space Craft Time

- This is a 32-bit counter with a will be a 16 second period counter. Its terminal count pin will connect to the RESET circuit. If the counter is not reset within the 16 sec period then RESET circuit will be activated, causing a "WARM-REBOOT" to occur.
- There will be a h/w register for STATUS/Control of the Watchdog circuit:
- Counter reset bit (WRITE)
- WARM-REBOOT Status (READ)
- Reset WARM-REBOOT Flag (WRITE)
- Enable/Disable Watchdog circuit (WRITE)

- Enable/Disable Watchdog Flag (READ)

5.4 Temperature & PSU Monitors - Board 3

The various ICU temperatures, voltages and currents are multiplexed into a single analogue line to the 8/10-bit ADC.

A TBD number of analogue signals will be connected to an analogue multiplexer. The single analogue output will feed to an 8-bit ADC.

The processor will be in control of the monitor circuit.

The signals to be monitored will be: TBD

Secondary 28V line: voltage and current

Secondary 5v line: voltage and current

ADSP-21020: temperature