Solar B – EIS

MULLARD SPACE SCIENCE LABORATORY

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FM ICU SC_PROC Design Definition

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CHANGE RECORD

ISSUE	DATE	PAGES CHANGED	COMMENTS
01	29 October 2001	All new	
02	24 June 2002		PFM design changes
03	15 February 2003		FM design changes

Table of Contents

1 Introduction

This document defines the Flight Model (FM) design of the processor board electronics (SC_PROC).

2 Applicable Documents

AD1: MSSL/SLB-EIS/SP010 PM ICU Hardware Design Definition

AD2: MSSL/SLB-EIS/SP003 Solar- B - EIS Interface Control Document

AD3: SLB-120 Solar-B Electrical Design Standard

AD4: MSSL/SLB-EIS/DD006 EIS ICU Software Architectural Design

AD5: MSSL/SLB-EIS/DD019 PM Camera/MHC Control Board Design Definition

AD6: MSSL/SLB-EIS/DD018 PM Monitor Board Design Definition

3 Space Craft Interface & Processor Card - (SC_PROC)

Data sheets for parts used to build the FM-SC_PROC card can be found on a CD-ROM.

The design is built around the TEMIC TSC21020F-20SB DSP running at 20MHZ.
All interface circuits are designed in RT54SX32-S Actels.

3.1 ICU Memory Specification

3.1.1 Program Memory SRAM

The part used is the Lockheed Martin 190A325-221– a 128k x 8-bit 25ns access speed 32 pin flat pack SRAM. This memory is set up as 48-bit wide connected to the “Program Memory” (PM) area of memory map. All PM area interfaces on the backplane (and thus on the buffered-side of the TBUS_CTL interface) are up to 16-bit wide. Data on these interfaces appear on bits: PMD[31:16]. See the address map later in this document for details of the memory organisation.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\LockheedMartin\128kSRAM-190a325f.pdf

3.1.2 Data Memory SRAM

The part used is the Lockheed Martin 190A325-221– a 128k x 8-bit 25ns access speed 32 pin flat pack SRAM. This memory is set up as 32-bit wide connected to the “Data Memory” (DM) area of memory map. All DM area interfaces on the backplane (and thus on the buffered-side of the TBUS_CTL interface) are up to 16-bit wide. Data on these interfaces appear on bits: DMD[23:8]. See the address map later in this document for details of the memory organisation.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\LockheedMartin\128kSRAM-190a325f.pdf

3.1.3 Boot PROM

The part used is the INTERSIL HS1-6664RH 8k x 8-bit PROM. This has a typical access speed of 35ns and is packaged as a 28pin 0.6" wide DIL I.C.

The PROM's are on the buffered-side of the TBUS_CTL interface, and are connected to the PM area on data bits PMD[23:16].

3.1.4 SC_I/F FIFO's

The part used is the TEMIC MMCP67204EV-30/883 4k x 9-bit with 30ns access speed.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\TEMIC\doc39745a1360452.pdf

3.2 Time/Watchdog/Interfaces & Boot Control FPGA (TWIB_CTL) – Actel_45

A RT54SX32S-CQ208BX3 208-pin Actel is used for all the main MDP interfaces and control units of the processor board.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Actels\RT54SX-Sv0.2\RT54SX-S.pdf

3.2.1 Command Interface – (CMD_IF) Detailed Design

The command interface state machine polls for serial data to be transmitted from the MDP. When the ENABLE signal is active data is clocked into a shift register by the CMD_CLK signal from the MDP. Bytes are latched and then written in parallel to three 4k x 9-bit FIFO's. On writing the last byte of a packet an interrupt is generated to the DSP.

The circuit uses bit-9 of the FIFO to add an End-of-Command (EOC) flag to the byte data. This is used by software to quickly determine the length of the incoming packet. Details of the interface timings and software protocols requirements for the CMD_IF are given in AD2.

The interface control software is detailed in AD4.

3.2.1.1 CMD_IF Status/Control Register – addr: 0xC0 0002

This is the full status/control register used for the CMD_I/F. The ~HF, ~EF, and ~FF flags are the OR function of the three FIFO's

PMD_x	D47	D46	D45	D44	D43	D42	D41	D40
RD:	0	~BitErr	~HF	~Irq	~OvrFlw	~EF	~FF	CMD_ENA
WR:	X	~ClrBitErr	X	~ClrIrq	~ClrOvrFlw	~RST	X	X

3.2.1.2 CMD_IF Status READ

PMD_x	Label	Description
d46	**~BitErr**	when at logic '0' it indicates an error in transmission: the packet was not a multiple of 8-bit bytes.
d45	**~HF**	'FIFO Half-Full Flag' – a logic '0' indicates the CMD_FIFO is at the half full boundary.
d44	**~Irq**	the active state is logic '0'. An interrupt is generated on the falling edge of the CMD_ENA signal.
d43	**~OvrFlw**	'FIFO Overflow Error' - if the CMD_FIFO is full when a new byte is ready to be written an overflow condition is indicated by this bit going active: logic '0'. The byte will be lost.
d42	**~EF**	'FIFO Empty Flag' – a logic '0' indicates the CMD_FIFO is empty.
d41	**~FF**	'FIFO Full Flag' - a logic '0' indicates the CMD_FIFO is full.
d40	**CMD_ENA**	when at logic '1' this signal indicates that the interface is active and that a packet is being transmitted.

3.2.1.3 CMD_IF Control WRITE

PMD_x	Label	Description
d46	**~ClrBitErr**	writing a logic '0' will clear the ~BIT_ERR condition to logic '1'
d44	**~ClrIrq**	writing a logic '0' will clear the current interrupt, and the ~Irq flag will be set to logic '1'
d43	**~ClrOvrFlw**	writing a logic '0' will clear the over-flow condition, and the ~OvrFlw flag is set to logic '1'
d42	**~RST**	writing a logic '0' will reset the CMD_I/F and CMD_FIFO

3.2.1.4 CMD_IF Data READ Register – addr: 0xC0 0003

Command packet data is read from the 27-bit wide CMD_FIFO from this address. Each 9-bit segment represents the 8-bit data byte plus 1-bit End-of-Packet (EOP) marker. Data format is as shown:

pmd47	pmd[46..39]	pmd38	pmd[37..30]	pmd29	pmd[28..21]	pmd[20..0]
EOP	fifo_d[7..0]	EOP	fifo_d[7..0]	EOP	fifo_d[7..0]	unused

3.2.2 Status Interface – (ST_IF) Detailed Design

The ST_IF FIFO uses a 4k x 9-bit FIFO. Only the lower 8-bits are used. The software writes a complete packet to the ST_FIFO as bytes. Then a "GO" instruction is sent to the ST_IF state machine and the packet data in the FIFO is automatically transmitted to the MDP.

As a status packet is only sent in response to a command, there is no need for additional hardware to generate interrupts or for software to poll the ST_IF STAT_REG.

Details of the interface timings and software protocols requirements for the ST_IF are given in AD2.

The interface control software is detailed in AD4.

3.2.2.1 ST_IF Status/Control Register – addr 0xC0 0004

This is the full status/control register used for the ST_I/F.

PMD_x	D47	D46	D45	D44	D43	D42	D41	D40
RD:	~ST_GO	0	0	0	0	~EF	~FF	ST_ENA
WR:	~ST_GO	X	X	X	X	~RST	X	X

3.2.2.2 ST_IF Status READ

PMD_x	Label	Description
d47	**~ST_GO**	this indicates the current condition of this flag. It initiates the start of the state machine which controls the interface. A logic '0' at PMD47 indicates when data from the ST_FIFO is being transmitted.
d42	**~EF**	'FIFO Empty Flag' – bit PMD42 is set to logic '0' when ST_FIFO is empty.
d41	**~FF**	'FIFO Full Flag' - bit PMD41 is set to logic '0' when the ST_FIFO is full.
d40	**ST_ENA**	when bit PMD40 is at logic '1' this signal indicates that the interface is active and that a packet is being transmitted.

3.2.2.3 ST_IF Control WRITE

PMD_x	Label	Description
d47	**~ST_GO**	once a packet has been loaded to the FIFO a logic '0' is written to bit PMD47. This starts the transmission of the data. This bit will automatically be set to logic '1' when the ST_FIFO goes empty.
d42	**~RST**	writing '0' to '0' to bit PMD42 will reset the ST_FIFO.

3.2.2.4 ST_IF Data WRITE Register – addr: 0xC0 0005

Status Data packet data is written to the 8-bit ST_FIFO at this address. Data format is as shown:

pmd[47..24]	pmd[23..16]
unused	fifo_d[7..0]

3.2.3 Mission Data Interface – (MD_IF) Detailed Design

The MD_IF FIFO is implemented as two 4k x 9-bit FIFO's connected in width expansion mode to give a 4k x 16-bit FIFO.

The MD_IF software task writes up to 4kword long sub-packets to the MD_FIFO. Once a sub-packet has been written to the MD_FIFO, the program issues a "GO" instruction to the MD_IF circuit. This will begin transmitting the packet when the BUSY signal is inactive.

Unlike the other interfaces the size of the Mission Data packet can be larger than the size of the MD_FIFO; to over come this limitation the packet is divided into sub-packets and the ~EOP (End of Packet) signal is used to hold the interface in a idle state whilst more data is written to the MD_FIFO.

The MD_IF hardware will issue an interrupt to the processor when the mission data packet has been sent.

Details of the interface timings and software protocols requirements for the MD_IF are given in AD2. The interface control software is detailed in AD4.

3.2.3.1 MD_IF Status/Control Register - addr: 0xC0 0006

This is the full status/control register used for the MD_I/F. The ~EF, and ~FF flags are the OR function of the two FIFO's

PMD_x	D47	D46	D45	D44	D43	D42	D41	D40
RD:	0	~FF	~EF	BSY	~IRQ	~EOP	~GO	0
WR:	~RST	X	X	X	~ClrIrq	~EOP	~GO	X

3.2.3.2 MD_IF Status READ

PMD_x	Label	Description
d46	**~FF**	'FIFO Full Flag' bit is set to logic '0' when MD_FIFO is full.
d45	**~EF**	'FIFO Empty Flag' bit is set to logic '0' when MD_FIFO is empty.
d44	**Bsy**	'BUSY' – this is the signal from the MDP which indicates when the MDP is still busy processing the last packet data. A logic '1' is the active level
d43	**~Irq**	an interrupt is generated when the final word of the packet has been transmitted as indicated by the falling edge of the MD_ENA signal. Bit PMD43 latches the state of the interrupt signal.
d42	**~EOP**	'End of Packet' – when this is set to '1' by the MD_I/F software task, it indicates that there are further sub-packets to transmit.
d41	**~MD_GO**	this is the current state of the ~GO bit. It initiates the start of the state machine which controls the interface. A logic '0' at PMD41 indicates when data from the MD_FIFO is being transmitted.

3.2.3.3 MD_IF Control WRITE

PMD_x	Label	Description
d47	**~RST**	writing logic '0' will reset the MD_I/F
d43	**~ClrIrq**	writing '0' to '0' will clear the interrupt to logic '1'.
d42	**~EOP**	'End of Packet' – set to logic '1' whilst transmitting **sub-packets**. After writing the **last sub-packet** to the MD_FIFO the **~GO** bit and **~EOP** are asserted (logic '0') to indicate the last sub-packet has been loaded. **Note – when altering other flags care should be taken not to corrupt this flag**.
d41	**~MD_GO**	after loading the MD_FIFO, writing logic '0' to this bit will start transmission of the data. This bit is automatically set to logic '1' when the MD_FIFO goes empty.

3.2.3.4 MD_IF Data WRITE Register – addr: 0xC0 0007

Mission Data packet data is written to the 16-bit MD_FIFO at this address. The data format is as shown:

pmd[47..39]	pmd[31..16]
unused	fifo_d[15..0]

3.2.4 Watchdog Interface Function

The Watchdog Timer function has a timer which can be enabled to give an initial time out period of approx. 7.78 seconds. A user register gives the option of changing this time-out period to be maximum of approx. 15.56 seconds.

By default the watchdog timer function is disabled and the watchdog timer is held in a reset (zero count) condition.

In operation the Terminal Count signal of the counter is connected to the RESET circuit. If the counter is not reset within the Time-out period, the RESET circuit will be activated, causing a Watchdog Trip (WARM-REBOOT) to occur: this has the effect of resetting all hardware to the initial "Power-ON" state, copying code from the PROM to RAM and running that code.

This Control/STATUS register is designed such that following a WARM-REBOOT, the global RESET signal is not applied to this register or the main clock generator circuit. Hence these register flags are preserved, giving the software an indication of what had happened.

The watchdog trigger signal has the following sources:

- watchdog counter – approx. 7.78 seconds or approx. 15.56 seconds – user selectable
- ~V_FAIL – a voltage sensor signal from the MON card

The interface control software is detailed in AD4.

3.2.4.1 WD_IF Status/Control Function - addr: 0xC0 0001

This is the full status/control register used for the WD_I/F.

PMD_x	D47	D46	D45	D44	D43	D42
RD:	~WDTrip	~WD_EN	~WDToSel	~V_Fail	~DC_Rst	0
WR:	~WDTripRst	~WD_EN	~WDToSel	~WD_RST	X	X

3.2.4.2 WD_IF Status Read

PMD_x	Label	Description
d47	**~WDTrip**	'Watchdog Trip' status – a logic '0' it indicates that a watchdog trip has occurred. On power-ON this is set to '1'.
d46	**~WD_EN**	'Watchdog Enable' status – a logic '0' indicates that the watchdog circuit is enabled. On power-ON this is set to '1'.
d45	**~WDToSel**	'Watchdog Time-Out Select' status – logic '0' selects a time-out period of approx. 15.56 sec. Logic '1' selects an approx. 7.78 sec. time-out period. On power-ON this is set to '1'.
d44	**~V_Fail**	If the voltage level is failing, this signal will be asserted to logic '0'. However, if all power is lost this (as the reset of the ICU) will loose all power, hence when the system is powered on this signal will be de-asserted to its initial condition (logic '1').
d43	**~DC_RST**	'Discrete Command Reset' status – a logic '0' indicates that a direct reset command was decoded. This flag is reset by writing to the **~WDTripRst** flag. On power-ON this is set to '1'.

3.2.4.3 WD_IF Control Write

PMD_x	Label	Description
d47	**~WDTripRst**	'Watchdog Trip Reset' – writing a logic '0' will de-assert the **~WD_Trip** & **~DC_RST** flags – i.e. set to logic '1'. On power-ON this is set to '1'.
d46	**~WD_EN**	'Watchdog Enable' – writing a logic '0' will enable the watchdog circuit. On power-ON this is set to '1' & circuit is disabled.
d45	**~WDToSel**	'Watchdog Time-Out Select' – writing a logic '0' selects the time-out period of approx. 15.56 seconds. With this bit set to '1' the time-out period selected is approx. 7.78 seconds. On power-ON this is set to '1'.
d44	**~WD_RST**	'Watchdog Reset' – writing a logic '0' will reset the watchdog counter only. **NOTE ~WDTrip** & **~DC_RST** flags or the rest of the watchdog circuit are **NOT** affected by this operation.

3.2.5 Space Craft Time Function

Space craft time is loaded into a 32-bit synchronous counter that is clocked by a 1.9531 ms period clock (f = 512.0065537 Hz). This gives an error in time of t_{err} = 2ns. EIS time is updated from the time value sent by the MDP with a command.

Details of time function requirements are given in AD2. exercises

3.2.5.1 SCTIME_IF Status READ – addr: 0xC0 0000

Time is read asynchronously as a 32-bit value from this address.

3.2.5.2 SCTIME_IF Control Write – addr: 0xC0 0000

Time is written asynchronously to as a 32-bit value to this address.

3.2.6 Discrete Hardware Reset (DC_RST) Function

When two single byte 0xF5 commands are issued within approximately 16 seconds a signal is sent to the watchdog circuit to cause a hardware reset. A ~DC_RST flag is updated to confirm the action.

3.3 Bus Control FPGA (TBUS_CTL) – Actel_46

A RT54SX32S-CQ208BX3 208-pin Actel is used to provide the processor bus retiming and buffering for slower/off board functions of the ICU. These include the 8k PROM, and all interface cards on the backplane. The interface allows 16-bit interfaces to be connected to it on PMD[31:16] and DMD[23:8].

The TBUS_CTL FPGA will automatically assert ~PMACK to the processor on a valid read/write cycle to the address space allocated to the slower/off board ports. If that device then asserts its ~PMACK_B signal within 2 processor clock cycles then the processor ~PMACK signal will be kept asserted until the ~PMACK_B signal from the device is removed. This allows individual devices to control the access time.

The TBUS_CTL FPGA gives a minimum cycle time of 200ns (four processor clock cycles).

3.4 Interrupts:

The table shows the source of each interrupt. The priority system for the DSP21020 is from ~IRQ3 to ~IRQ0; with ~IRQ3 being the highest priority.

~IRQ3	CMD_IF	interrupt on reception of a full command packet.
~IRQ2	MHC	interrupt on reception of byte on the UART.
~IRQ1	ROE	interrupt on reception of byte on the UART.
~IRQ0	MD_IF	interrupt on transmission of final word of sub-packet.

3.5 Boot Function FPGA - (Boot_Ctl)

In the EIS ICU a default set of program code, data, tables, and sequences are stored in non-volatile PROM's and EEPROM's.

In 48-bit long instructions are stored in PROM's in a serial byte format. At POWER-ON, or during a WARM_REBOOT, the Boot_Ctl FPGA holds the DSP in a RESET condition whilst reading six bytes at a time from the PROM starting at address **0x00 0000**. The six byte instruction formed can then be written to Program RAM from address **0x00 0000**. The next six bytes are read from PROM (which is from address **0x00 0005**) and written to Program RAM address **0x00 0001**. In this manner a very small "Boot-Loader" program is copied from PROM to RAM. Then the DSP RESET line is released and the DSP starts execution of the code copied to RAM.

3.6 MDP-ICU Interface Differential Driver Circuits

Details of the interface circuit requirements between the ICU and MDP are in AD2.

3.7 Test Connectors

Two test connectors are provided on the SC_PROC board:

3.7.1 OD Test Port

A 40-way IDC header is provided for test debugging. This provides the un-buffered signals **PMD[47:16]**, **~WRM_RST, ~OD0, GND** and **VDD.** The **~OD0** signal is a decoded user port. Software can write 32-bit data to these addresses. These signals go to a test circuit which buffers the data bus to a FIFO. The FIFO data is then transmitted to a PC via standard RS-232 UART interface. The **~WRM_RST** allows the test circuit FIFO's to be reset when ever the ICU is reset. **~OD0** is used to latch data bits **PMD[47:16]** on the test board;

3.7.2 JTAG Port

This port allows programs to be downloaded to memory, programs to be single-stepped, and DSP registers to be observed.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Processor\Temic21020f.pdf and Analog Devices ADSP-21020 User Manual.

4 PM_ICU Memory Map

4.1 Program Memory Space

Memory Bank		Physical Address	PMA[23,22,21]
Bank 0 (PMS0*)	Program RAM	0x00 0000 128k * 48-bit RAM 0 wait states 0x01 FFFF	000
Bank 1 (PMS1*)	Not Used	0x20 0000 0x7F FFFF	000
	CM_Ctl I/O Ports	0x80 0000 h/w & s/w defined wait states 0x8B FFFF	100
	Not Used	0x8C 0000 0x9F FFFF	100
	MON I/O Ports	0xA0 0000 3 wait states 0xA0 000F	101
	Not Used	0xA0 0010 0xBF FFFF	101
	SC_PROC I/O Ports	0xC0 0000 3 wait states 0xCF FFFF	110
	PROM	0xE0 0000 32k * 8-bit PROM 3 wait states 0xE0 7FFF	111

4.2 Data Memory Space

Memory Bank		Physical Address
Bank 0 (DMS0*)	Data RAM	0x0000 0000 128k * 32-bit RAM 0 wait states 0x0001 FFFF
Bank 1 (DMS1*)	CCD Buffer	0x0100 0000 2M * 16-bit RAM H/W wait states 0x011F FFFF NOTE: Buf_A & Buf _B occupy the same address space.
Bank 2 (DMS2*)	Not Used	0x0200 0000 0x020F FFFF
Bank 3 (DMS3*)	EEPROM	0x0300 0000 1M * 8-bit EEPROM (8 off) H/W wait states 0x030F FFFF
	Not Used	0x0310 0000 0xFFFF FFFF (top of Data space)

4.3 PM_ICU I/O Port Map – Program Memory (Bank 1) - PMS1*

Base Address		Function: address(HEX)	Port Name	Note
PMA				
[23:21]	[3:0]	**Space Craft Time IF: 0xC0 0000**		32-bit counter
11x	0000	SCTIME Control Register	SCTIME_WR	Load new time value from Space Craft
	0000		SCTIME_RD	Read current time value
		Watchdog IF: 0xC0 0001		approx. 7/15sec time-out circuit
	0001	WATCHDOG Control Reg.	WATCHDOG_CTL_WR	Counter RESET, EN/DISABLE
	0001	Read WATCHDOG Status	WATCHDOG_STAT_RD	WatchDog trip status etc.
		Command IF: 0xC0 0002		
	0010	CMD Control Register	CMD_CTL_WR	Reset, Read from FIFO, interrupt etc
	0010	CMD Status Register	CMD_STAT_RD	Status information register
		Command IF: 0xC0 0003		
	0011	Read CMD Buffer Data	CMDDATA_RD	8-bit port from FIFO buffer
		Status IF: 0xC0 0004		
	0100	ST Control Register	ST_CTL_WR	Reset, Write to FIFO, etc
	0100	ST Status Register	ST_STAT_RD	Status information register
		Status IF: 0xC0 0005		
	0101	Write Data to ST Buffer	STDATA_WR	8-bit data port to FIFO buffer
		Mission Data IF: 0xC0 0006		
	0110	MD Control Register	MD_CTL_WR	Reset, Write to FIFO, etc
	0110	MD Status Register	MD_STAT_RD	Status information register
		Mission Data IF: 0xC0 0007		
	0111	Write Data to MD Buffer	MDDATA_WR	16-bit port to FIFO buffer
		Odmeter IF: 0xC0 0008		
	1000	Write Data to OD port #0	OD0_WR	Latch 32-bit value to HEX display
		Odmeter IF: 0xC0 0009		
	1001	Write Data to OD port #1	OD1_WR	Latch 32-bit value to HEX display
		Free Address:		
	1010			
	to	spare	spare	
	1111			
100	xxxx	**CM_Ctl: 0x80 000x**		
	see AD5	Camera/MHC Control Registers	see AD5	see AD5
	see AD5	High Speed Link Control Registers	see AD5	see AD5
101	xxxx	**PSU Monitor IF: 0xA0 000x**		
see AD6	see AD6	PSU Monitor Control	see AD6	see AD6
		Free Address:		
	0010			
	to	spare	spare	
	1111			

PMA[20:4] = don't care.

5 Schematics

Drawing Number:

5275/009-5	Issue 1.1

Hierarchical list of sheets:

FM_ICU.1	Issue 1.0
SC_PROC.1	13/12/2002
DSP.1	25/09/2002
DAT_RAM.1	18/03/2002
PRG_RAM.1	18/03/2002
TWIB_CTL.1	03/10/2002
TTWIB_CTL.1	08/04/2002
ACTEL_45.1	04/07/2002-TBD
TBUS_CTL.1	13/12/2002
TTBUS_CTL.1	08/07/2002
ACTEL_46.1	30/08/2002

6 Actel FPGA Programming Information

6.1 TWIB_CTL Actel

The design files for FPGA TWIB_CTL are in the CD-ROM directory:

\Designs\Solar-B\FM_ICU.1v1\Actels\Actel_45\

The part programmed is:

TWIB_CTL – A54SX32A-PQ208 – v1.3

signature: TBD

user ID: TBD

check sum: TBD

dev sum: TBD

The device was programmed using the DOS version of Silicon Sculptor: DOS3.54 – 04/02/01 from laptop mssllkr-2

6.2 TBUS_CTL Actel

The design files for FPGA TBUS_CTL are in the CD-ROM directory:

\Designs\Solar-B\FM_ICU.1v1\Actels\Actel_46\

The part programmed is:

TBUS_CTL – A54SX32A-PQ208 – v1.0

signature: TBD

user ID: TBD

check sum: TBD

dev sum: TBD

The device was programmed using the DOS version of Silicon Sculptor: DOS3.54 – 04/02/01 from laptop mssllkr-2

7 PCB Manufacturing and Board Assembly and Parts List

Drawing Number:

A1/5275/009-5	assembly drawing and parts list	Issue 3
X-1639-003	pcb	

Mechanical Drawing:

A1/5275/303-16	SC_PROC Board Profile	Issue 5

8 Bill of Materials

Generated from Viewlogic design for SC_PROC.1:

SC_PROC.LST 13/10/2002

See **section 11** for parts list with flight part numbers. Note the parts list give is a hand-edited version of this list.

9 Construction Operations

9.1 Notes

Take note of the **orientation of components:**

I.C.'s **DO NOT** flow in one direction

Resistors: vertically mounted – shall be placed as shown on the assembly drawing. The wire leg is used for test measurements.

9.2 Links

- Connect signals for unused gates to **GND**:

  close:

  J5 – on inverter U41

  J6 – on inverter U41

  J7 – on inverter U41

  J8 – on differential driver U37

  J9 – on differential driver U36

  J10 – on inverter U41

- Connect signal '**COM**' to p.c.b. **GND** signal:

  close: J2

- Connect Actel_45 (TWIB_CTL) user I/O signals '**CLKB_OUT**' (o/p) to '**CLK_B**' (i/p):

  close: J11

- Select PROM boot operation via link LS1:

  close: LS1 – wire link from 1->2

- Configure JTAG port (LK1) as follows:

  close:

  5 and 6: TCLK

  7 and 8: ~TRST

  11 and 12: TDO

9.3 Select on Test Items

none.

9.4 Modifications

Check ECR's for latest modifications to board.

- Connect:

  OVERALL_SCN0:X1 to screw-lock

  OVERALL_SCN1':X2 to screw-lock

- Use pins for test connector whilst testing FM card:

  TST-CON:CN2

- Add a RESET push-to-make switch during FM testing:

  wire across J3 and route to front panel

- Only add the following test points:

  GND: X18, X19, X20, X21, X22, X23, X24, X25, X26, X27, X31, X32, X141, X142, X143, X144, X145, X146, X147, X148, X156.

10 Layout Instructions

10.1 Input to Mentor

Files are generated from a Viewlogic conversion utility to mentor format.

NO modifications allowed to COMPS_FILE or NETS_FILE without permission from **RAC**.

Filename & path	**Description**
~\Designs\Solar-B\FM_ICU.1v1\	Viewlogic FM_ICU SC_PROC design directory
~\Apps\WV7.53\STANDARD **mentor.cfg**	Viewlogic netlister configuration control file for Mentor system
~\Designs\Solar-B\FM_ICU.1v1 \ men_SC_PROC**comps_file.cmps**	Viewlogic component packages file
~\Designs\Solar-B\FM_ICU.1v1 \ men_SC_PROC**nets_file.net**	Viewlogic design netlist file

11 Parts List

sc_proc **Thursday, October 3, 2002 5:38 pm**

SOLAR-B: FM ICU

REVISION_HISTORY:

1 05/07/2002 ORIGINAL
1. 25/09/2002 SYSCLK/RST-ACT_46, MOD ACTEL-
1 JTAG

#	QTY	REFDES	Flight Part #	DEVICE	VALUE	PKG_TYPE	PART_SPEC
1	2	C1,C2	CWR11MH105KC	SMC_POL_CAP	10UF/25V	CWR11_D	SMC_POL_CAP
2	31	C6,C7,C8,C9,C12, C13,C14,C15,C42, C43,C44,C45,C46, C47,C50,C51,C52, C53,C57,C59,C60, C61,C62,C63,C68, C69,C70,C71,C75, C76,C77	CDR32BX103BKWS	SM_CAPACITOR_1206	10NF	1206	SM_CAPACITOR_1206
3	22	C10,C11,C28,C29, C30,C31,C32,C33, C34,C35,C36,C37, C38,C39,C40,C41, C48,C49,C54,C58, C66,C67	CDR33BX104AKWS	SM_CAPACITOR_1210	100NF	1210	SM_CAPACITOR_1210
4	1	C27	CDR32BP101BJWS	SM_CAPACITOR_1206	100PF	1206	SM_CAPACITOR_1206
5	1	CN1	DBM25S511NMB	DFRA25_BKT		DBM25S_1A7N	D-TYPE 25-W-R/A FEMALE_BRKT

6	1	CN2	HEADER2X20	HEADER2X20		HEADER_2X20WAY	HEADER_40WAY_MALE_STRAIGHT
7	1	D1	JANTXV1N4148	1N4148	1N4148	DO35	1N4148 DIODE
8	11	J1,J2,J3,J4,J5,J6, J7,J8,J9,J10,J11	2-PIN_JUMPER	2-PIN_JUMPER		HEADER_2WAY	0.1 PITCH LINK
~~9~~	~~1~~	~~LK1~~		~~HEADER6X2~~		~~HEADER_2X6WAY~~	~~2X6 BLOCK OF LINKS~~
10	1	LS1	3-WAY_JUMPER	3-WAY_JUMPER		HEADER_1X3WAY	ONE TWO POSITION LINK
11	2	P0,P1	HPF098UMBKO070			HPF098AMBK0020	HYPERTAC 98-WAY R/ANGLE MALE
12	14	R1,R2,R17,R18,R19, R20,R21,R23,R166, R167,R168,R169, R170,R171	RLR05C1000GS	RLR05_VERTICAL	100R	RLR05_V	RESISTOR_RLR05_VERTICAL
13	13	R3,R4,R5,R8,R9,R10, R11,R12,R67,R71, R72,R97,R98	RLR05C4751FS	RLR05_VERTICAL	4K7	RLR05_V	RESISTOR_RLR05_VERTICAL
14	6	R6,R7,R13,R14,R15, R16	RLR05C0330GS	RLR05_VERTICAL	33R	RLR05_V	RESISTOR_RLR05_VERTICAL
15	6	R22,R26,R27,R94, R95,R96	RLR05C1002FS	RLR05_VERTICAL	10K	RLR05_V	RESISTOR_RLR05_VERTICAL
16	1	R24	RLR05C1003FS	RLR05_VERTICAL	100K	RLR05_V	RESISTOR_RLR05_VERTICAL
17	1	R25	RLR05C2203GS	RLR05_VERTICAL	220K	RLR05_V	RESISTOR_RLR05_VERTICAL

#	**QTY**	**REFDES**	**Flight Part #**	**DEVICE**	**VALUE**	**PKG_TYPE**	**PART_SPEC**
18	107	R28,R29,R30,R31, R32,R33,R34,R35, R36,R37,R38,R39, R40,R41,R42,R43, R44,R45,R46,R47, R48,R49,R50,R51, R52,R53,R54,R55, R56,R57,R58,R59, R60,R61,R62,R64, R68,R73,R74,R75, R76,R77,R78,R84,	RLR05C47R5FS	RLR05_VERTICAL	47R	RLR05_V	RESISTOR_RLR05_VERTICAL

		R85,R86,R87,R88, R91,R108,R109,R110, R111,R112,R113, R114,R115,R116, R117,R118,R119, R121,R122,R123, R124,R125,R126, R127,R128,R129, R130,R131,R132, R133,R134,R135, R136,R137,R138, R139,R140,R141, R142,R143,R144, R145,R146,R147, R148,R149,R150, R151,R152,R153, R154,R155,R156, R157,R158,R159, R160,R161,R162, R163,R164,R177,R181					
19	19	R65,R66,R69,R70, R79,R80,R81,R82, R83,R89,R90,R92, R93,R165,R172,R173, R174,R175,R182	RLR05C2202GS	RLR05_VERTICAL	22K	RLR05_V	RESISTOR_RLR05_VERTICAL
20	1	R120	RLR05C1801GS	RLR05_VERTICAL	1K8	RLR05_V	RESISTOR_RLR05_VERTICAL
21	2	R179,R180	RLR05C1001GS	RLR05_VERTICAL	1K	RLR05_V	RESISTOR_RLR05_VERTICAL
22	8	RS1,RS2,RS7,RS8, RS9,RS10,RS11,RS12	M8340106K4701GC	8_RESISTOR_SIL	4K7	SIL9	8_RESISTOR_SIL
23	4	RS3,RS4,RS5,RS6	M8340106M2002GC	8_RESISTOR_SIL	22K	SIL9	8_RESISTOR_SIL
24	1	T1	311P18-7057R6	311P18-7057R6	10K	YSI_44900_TYPES-S	YSI_THERMISTOR
25	1	U1	ACTEL_45	ACTEL_45	TWIB_CTL	CQPQ208_IN_SKT	A54SX32S_208_PINOUT
26	1	U2	5962F9568901QXC	26C32_FP		FPSO16_DUAL	QUAD DIFF_RX_DUAL_FP

#	QTY	REFDES	Flight Part #	DEVICE	VALUE	PKG_TYPE	PART_SPEC
27	6	U3 U4 U5 U6 U7 U8	MMCP67204EV-30/883	M67204	4K_FIFO	DIP28_C	ATMEL 4K*9 ASYNC FIFO-CP300MIL
28	1	U9	ACTEL_46	ACTEL_46	BUS_CTL	CQPQ208_IN_SKT	A54SX32S_208_PINOUT
29	2	U10 U21	XMIG000301BF	HS1-6664RHT	8K_PROM	DIP28W_C	INTERSIL DIL28-0.6_8K PROM
30	10	U11 U12 U13 U14 U15 U16 U17 U18 U19 U20	5962H9687705VYC	LMFS1024_234	128K_SRAM	CFP32_0.65	LM 128K SRAM-32-PIN WIDE FP
31	1	U25	TSC21020F-20SB	TSC21020F	21020_DSP	MQFP256	TEMIC TSC21020F-20SB
32	2	U36 U37	5962F9666301QXC	26C31_FP2		FPSO16_DUAL	QUAD DIFF_RX_DUAL_FP
33	1	U41	940900703CF	54HC14		DIP14	SCHMITT HEX INVERTER
34	87	X1,X2,X3,X4,X5,X6, X7,X8,X9,X10,X11, X12,X13,X14,X15, X16,X17,X18,X19, X20,X21,X22,X23, X24,X25,X26,X27, X28,X29,X30,X31, X32,X33,X34,X35, X36,X38,X39,X41, X42,X43,X44,X45,		TEST_POINT		C063_PAD	TEST POINT

		X46,X47,X115,X116,					
		X117,X118,X119,					
		X120,X123,X124,					
		X125,X126,X131,					
		X132,X133,X134,					
		X135,X136,X137,					
		X138,X139,X140,					
		X141,X142,X143,					
		X144,X145,X146,					
		X147,X148,X149,					
		X150,X151,X152,					
		X153,X154,X155,					
		X156,X157,X158,					
		X159,X160,X161,X162					
35	1	XT1	MCM 4132-1M		20MHZ	QT6	ACMOS 5V OSCILLATOR

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