Solar B – EIS

MULLARD SPACE SCIENCE LABORATORY

UNIVERSITY COLLEGE LONDON **Author: R. A. Chaudery**

PM ICU Design Definition

Document Number: MSSL/SLB-EIS/DD/012.01

Distribution:

NRL	G Doschek	
	C Korendyke	
	S Myers	
	C Brown	
	K Dere	
	J Mariska	
NAOJ	H Hara	
	T Watanabe	
RAL	J Lang	
	B Kent	
BU	C Castelli	
	S Mahmoud	
Mullard Space Science Laboratory	J L Culhane	
	A Smith	
	A James	
	L Harra	.
	A McCalden	
	C McFee	
	R Chaudery	
	P Thomas	
	R Card	
	B Winter	
	P Coker	
	R Gowen	
	K Al Janabi	
	M Whillock	
SLB-EIS Project Office	A Dibbens	Orig

Author: Date:

Authorised By Date:

Distributed: Date:

CHANGE RECORD

ISSUE	DATE	PAGES CHANGED	COMMENTS
01	29 October 2001	All new	

Table of Contents

1 Introduction

This document defines the design of the processor board electronics (SC_PROC) for the Proto Model of the ICU (PM_ICU).

2 Applicable Documents

AD1: MSSL/SLB-EIS/SP010 PM ICU Hardware Design Definition

AD2: MSSL/SLB-EIS/SP003 Solar- B - EIS Interface Control Document

AD3: SLB-120 Solar-B Electrical Design Standard

AD4: MSSL/SLB-EIS/DD006 EIS ICU Software Architectural Design

AD5: MSSL/SLB-EIS/DD019 PM Camera/MHC Control Board Design Definition

AD6: MSSL/SLB-EIS/DD018 PM Monitor Board Design Definition

3 Space Craft Interface & Processor Card - (SC_PROC)

The SC_PROC board has been designed to be as close to the flight model as possible. For the production of the SC_PROC p.c.b. the device and package names (as listed in the parts list) are flight representative part references. Some components are not available with the same package or pinout in commercial versions. For these, parts with compatible specifications have been used, and then wire links have been used to solder the part to the FM p.c.b. foot-print layout.

The following sections describes the major components of the SC_PROC and references the parts that have been substituted for those listed in the parts list.

3.1 21020 DSP

The SC_PROC board uses the TEMIC TSC21020F-20SB DSP. This is the engineering version of the flight DSP, and as such is in the same 256-pin MQFP package and has the same timing specification as for flight.

The ICU runs at 20 MHz.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Processor\Temic21020f.pdf

3.2 ICU Memory Specification

3.2.1 Program Memory SRAM

The part used is the ISSI IS61C1024-20J – a 128k x 8-bit 25ns access speed 300-mil SOJ package SRAM. This part has a different footprint to the flight part in that the width of the part is narrower. As such extension wires have been soldered from one side of the I.C. to the track pads.

For the PM_ICU the program SRAM is set to run with 3 wait states for access.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\ISIS\61C1024L.pdf

3.2.2 Data Memory SRAM

The part used is the ISSI IS61C1024-20J – a 128k x 8-bit 25ns access speed 300-mil SOJ package SRAM. This part has a different footprint to the flight part in that the width of the part is narrower. As such extension wires have been soldered from one side of the I.C. to the track pads.

For the PM_ICU the program SRAM is set to run with 3 wait states for access.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\ISIS\61C1024L.pdf

3.2.3 Working Memory SRAM

The part used is the UTMC 512k by 8-bit UT7Q512-UPC I.C. with 100ns access speed. This is an engineering quality part, with no screening. This particular part's footprint differs from the flight part: it is housed as a 32-pin ceramic flat pack and the pinout differs. Wiring modifications are required to solder this part onto the p.c.b.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\Aeroflex\512k SRAM\7Q512sram.pdf

3.2.4 Boot PROM

For the PM_ICU the ATMEL AT28C256B-25PC (64k x 8-bit) EEPROM is used.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\ATMEL \ AT28C256.pdf

3.2.5 SC_I/F FIFO's

The part used is the IDT7204L35TP 4k x 9-bit with 35ns access speed.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Memory\IDT\7204.pdf

3.3 Time/Watchdog/Interfaces & Boot Control FPGA (TWIB_CTL)

A single A54SX32 208-pin Actel is used for all the main MDP interfaces and control units of the processor board. For the PM_ICU the Actel FPGA is put in a socket.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Actels\v1.1-data sheet \54SXSRTDS_041800.pdf – 54SXA32 Actel data sheet.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Actels\sy-208 socket\sy-pq208a.pdf – socket details.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Actels\sy-208 socket\sy-pq208b.pdf – pcb layout for socket.

3.3.1 Command Interface – (CMD_IF) Detailed Design

The command interface state machine polls for serial data to be transmitted from the MDP. When the ENABLE signal is active data is clocked into a shift register by the CMD_CLK signal from the MDP. Bytes are latched and then written in parallel to three 4k x 9-bit FIFO's. On writing the last byte of a packet an interrupt is generated to the DSP.

The circuit uses bit-9 of the FIFO to add an End-of-Command (EOC) flag to the byte data. This is used by software to quickly determine the length of the incoming packet. Details of the interface timings and software protocols requirements for the CMD_IF are given in AD2.

The interface control software is detailed in AD4.

3.3.1.1 CMD_IF Status/Control Register – addr: 0xC0 0002

This is the full status/control register used for the CMD_I/F. The ~HF, ~EF, and ~FF flags are the OR function of the three FIFO's

PMD_x	D47	D46	D45	D44	D43	D42	D41	D40
RD:	0	~BitErr	~HF	~Irq	~OvrFlw	~EF	~FF	CMD_ENA
WR:	X	~ClrBitErr	X	~ClrIrq	~ClrOvrFlw	~RST	X	X

3.3.1.2 CMD_IF Status READ

PMD_x	Label	Description
d46	**~BitErr**	when at logic '0' it indicates an error in transmission: the packet was not a multiple of 8-bit bytes.
d45	**~HF**	'FIFO Half-Full Flag' – a logic '0' indicates the CMD_FIFO is at the half full boundary.
d44	**~Irq**	the active state is logic '0'. An interrupt is generated on the falling edge of the CMD_ENA signal.
d43	**~OvrFlw**	'FIFO Overflow Error' - if the CMD_FIFO is full when a new byte is ready to be written an overflow condition is indicated by this bit going active: logic '0'. The byte will be lost.
d42	**~EF**	'FIFO Empty Flag' – a logic '0' indicates the CMD_FIFO is empty.
d41	**~FF**	'FIFO Full Flag' - a logic '0' indicates the CMD_FIFO is full.
d40	**CMD_ENA**	when at logic '1' this signal indicates that the interface is active and that a packet is being transmitted.

3.3.1.3 CMD_IF Control WRITE

PMD_x	Label	Description
d46	**~ClrBitErr**	writing a logic '0' will clear the ~BIT_ERR condition to logic '1'
d44	**~ClrIrq**	writing a logic '0' will clear the current interrupt, and the ~Irq flag will be set to logic '1'
d43	**~ClrOvrFlw**	writing a logic '0' will clear the over-flow condition, and the ~OvrFlw flag is set to logic '1'
d42	**~RST**	writing a logic '0' will reset the CMD_I/F and CMD_FIFO

3.3.1.4 CMD_IF Data READ Register – addr: 0xC0 0003

Command packet data is read from the 27-bit wide CMD_FIFO from this address. Each 9-bit segment represents the 8-bit data byte plus 1-bit End-of-Packet (EOP) marker. Data format is as shown:

pmd47	pmd[46..39]	pmd38	pmd[37..30]	pmd29	pmd[28..21]	pmd[20..0]
EOP	fifo_d[7..0]	EOP	fifo_d[7..0]	EOP	fifo_d[7..0]	unused

3.3.2 Status Interface – (ST_IF) Detailed Design

The ST_IF FIFO uses a 4k x 9-bit FIFO. Only the lower 8-bits are used. The software writes a complete packet to the ST_FIFO as bytes. Then a "GO" instruction is sent to the ST_IF state machine and the packet data in the FIFO is automatically transmitted to the MDP.

As a status packet is only sent in response to a command, there is no need for additional hardware to generate interrupts or for software to poll the ST_IF STAT_REG.

Details of the interface timings and software protocols requirements for the ST_IF are given in AD2.

The interface control software is detailed in AD4.

3.3.2.1 ST_IF Status/Control Register – addr 0xC0 0004

This is the full status/control register used for the ST_I/F.

PMD_x	D47	D46	D45	D44	D43	D42	D41	D40
RD:	~ST_GO	0	0	0	0	~EF	~FF	ST_ENA
WR:	~ST_GO	X	X	X	X	~RST	X	X

3.3.2.2 ST_IF Status READ

PMD_x	Label	Description
d47	**~ST_GO**	this indicates the current condition of this flag. It initiates the start of the state machine which controls the interface. A logic '0' at PMD47 indicates when data from the ST_FIFO is being transmitted.
d42	**~EF**	'FIFO Empty Flag' – bit PMD42 is set to logic '0' when ST_FIFO is empty.
d41	**~FF**	'FIFO Full Flag' - bit PMD41 is set to logic '0' when the ST_FIFO is full.
d40	**ST_ENA**	when bit PMD40 is at logic '1' this signal indicates that the interface is active and that a packet is being transmitted.

3.3.2.3 ST_IF Control WRITE

PMD_x	Label	Description
d47	**~ST_GO**	once a packet has been loaded to the FIFO a logic '0' is written to bit PMD47. This starts the transmission of the data. This bit will automatically be set to logic '1' when the ST_FIFO goes empty.
d42	**~RST**	writing '0' to '0' to bit PMD42 will reset the ST_FIFO.

3.3.2.4 ST_IF Data WRITE Register – addr: 0xC0 0005

Status Data packet data is written to the 8-bit ST_FIFO at this address. Data format is as shown:

pmd[47..24]	pmd[23..16]
unused	fifo_d[7..0]

3.3.3 Mission Data Interface – (MD_IF) Detailed Design

The MD_IF FIFO is implemented as two 4k x 9-bit FIFO's connected in width expansion mode to give a 4k x 16-bit FIFO.

The MD_IF software task writes up to 4kword long sub-packets to the MD_FIFO. Once a sub-packet has been written to the MD_FIFO, the program issues a "GO" instruction to the MD_IF circuit. This will begin transmitting the packet when the BUSY signal is inactive.

Unlike the other interfaces the size of the Mission Data packet can be larger than the size of the MD_FIFO; to over come this limitation the packet is divided into sub-packets and the ~EOP (End of Packet) signal is used to hold the interface in a idle state whilst more data is written to the MD_FIFO.

The MD_IF hardware will issue an interrupt to the processor when the mission data packet has been sent.

Details of the interface timings and software protocols requirements for the MD_IF are given in AD2. The interface control software is detailed in AD4.

3.3.3.1 MD_IF Status/Control Register - addr: 0xC0 0006

This is the full status/control register used for the MD_I/F. The ~EF, and ~FF flags are the OR function of the two FIFO's

PMD_x	D47	D46	D45	D44	D43	D42	D41	D40
RD:	0	~FF	~EF	BSY	~IRQ	~EOP	~GO	0
WR:	~RST	X	X	X	~ClrIrq	~EOP	~GO	X

3.3.3.2 MD_IF Status READ

PMD_x	Label	Description
d46	**~FF**	'FIFO Full Flag' bit is set to logic '0' when MD_FIFO is full.
d45	**~EF**	'FIFO Empty Flag' bit is set to logic '0' when MD_FIFO is empty.
d44	**Bsy**	'BUSY' – this is the signal from the MDP which indicates when the MDP is still busy processing the last packet data. A logic '1' is the active level
d43	**~Irq**	an interrupt is generated when the final word of the packet has been transmitted as indicated by the falling edge of the MD_ENA signal. Bit PMD43 latches the state of the interrupt signal.
d42	**~EOP**	'End of Packet' – when this is set to '1' by the MD_I/F software task, it indicates that there are further sub-packets to transmit.
d41	**~MD_GO**	this is the current state of the ~GO bit. It initiates the start of the state machine which controls the interface. A logic '0' at PMD41 indicates when data from the MD_FIFO is being transmitted.

3.3.3.3 MD_IF Control WRITE

PMD_x	Label	Description
d47	**~RST**	writing logic ‘0’ will reset the MD_I/F
d43	**~ClrIrq**	writing ‘0’ to ‘0’ will clear the interrupt to logic ‘1’.
d42	**~EOP**	‘End of Packet’ – set to logic ‘1’ whilst transmitting **sub-packets**. After writing the **last sub-packet** to the MD_FIFO the **~GO** bit and **~EOP** are asserted (logic ‘0’) to indicate the last sub-packet has been loaded. **Note – when altering other flags care should be taken not to corrupt this flag**.
d41	**~MD_GO**	after loading the MD_FIFO, writing logic ‘0’ to this bit will start transmission of the data. This bit is automatically set to logic ‘1’ when the MD_FIFO goes empty.

3.3.3.4 MD_IF Data WRITE Register – addr: 0xC0 0007

Mission Data packet data is written to the 16-bit MD_FIFO at this address. The data format is as shown:

pmd[47..39]	pmd[31..16]
unused	fifo_d[15..0]

3.3.4 Watchdog Interface Function

The Watchdog Timer function has a timer which can be enabled to give an initial time out period of approx. 7.78 seconds. A user register gives the option of changing this time-out period to be maximum of approx. 15.56 seconds.

By default the watchdog timer function is disabled and the watchdog timer is held in a reset (zero count) condition.

In operation the Terminal Count signal of the counter is connected to the RESET circuit. If the counter is not reset within the Time-out period, the RESET circuit will be activated, causing a Watchdog Trip (WARM-REBOOT) to occur: this has the effect of resetting all hardware to the initial “Power-ON” state, copying code from the PROM to RAM and running that code.

This Control/STATUS register is designed such that following a WARM-REBOOT, the global RESET signal is not applied to this register or the main clock generator circuit. Hence these register flags are preserved, giving the software an indication of what had happened.

The watchdog trigger signal has the following sources:

- watchdog counter – approx. 7.78 seconds or approx. 15.56 seconds – user selectable
- ~V_FAIL – a voltage sensor signal from the MON card

The interface control software is detailed in AD4.

3.3.4.1 WD_IF Status/Control Function - addr: 0xC0 0001

This is the full status/control register used for the WD_I/F.

PMD_x	D47	D46	D45	D44	D43	D42
RD:	~WDTrip	~WD_EN	~WDToSel	0	~DC_Rst	0
WR:	~WDTripRst	~WD_EN	~WDToSel	~WD_RST	X	X

Note: **PMD_42** will be utilised for the **'~V_Fail'** flag in the FM_ICU design.

3.3.4.2 WD_IF Status Read

PMD_x	Label	Description
d47	**~WDTrip**	'Watchdog Trip' status – a logic '0' it indicates that a watchdog trip has occurred. On power-ON this is set to '1'.
d46	**~WD_EN**	'Watchdog Enable' status – a logic '0' indicates that the watchdog circuit is enabled. On power-ON this is set to '1'.
d45	**~WDToSel**	'Watchdog Time-Out Select' status – logic '0' selects a time-out period of approx. 15.56 sec. Logic '1' selects an approx. 7.78 sec. time-out period. On power-ON this is set to '1'.
d43	**~DC_RST**	'Direct Command Reset' status – a logic '0' indicates that a direct reset command was decoded. This flag is reset by writing to the **~WDTripRst** flag. On power-ON this is set to '1'.

3.3.4.3 WD_IF Control Write

PMD_x	Label	Description
d47	**~WDTripRst**	'Watchdog Trip Reset' – writing a logic '0' will reset the **~WD_Trip** & **~DC_RST** flags. On power-ON this is set to '1'.
d46	**~WD_EN**	'Watchdog Enable' – writing a logic '0' will enable the watchdog circuit. On power-ON this is set to '1' & circuit is disabled.
d45	**~WDToSel**	'Watchdog Time-Out Select' – writing a logic '0' selects the time-out period of approx. 15.56 seconds. With this bit set to '1' the time-out period selected is approx. 7.78 seconds. On power-ON this is set to '1'.
d44	**~WD_RST**	'Watchdog Reset' – writing a logic '0' will reset the watchdog counter only. **NOTE ~WDTrip** & **~DC_RST** flags or the rest of the watchdog circuit are **NOT** affected by this operation.

3.3.5 Space Craft Time Function

Space craft time is loaded into a 32-bit synchronous counter that is clocked by a 1.9 ms period clock. EIS time is updated from the time value sent by the MDP with a command.

Details of time function requirements are given in AD2. exercises

3.3.5.1 SCTIME_IF Status READ – addr: 0xC0 0000

Time is read asynchronously as a 32-bit value from this address.

3.3.5.2 SCTIME_IF Control Write – addr: 0xC0 0000

Time is written asynchronously to as a 32-bit value to this address.

3.4 Interrupts:

The table shows the source of each interrupt. The priority system for the DSP21020 is from ~IRQ3 to ~IRQ0; with ~IRQ3 being the highest priority.

~IRQ3	CMD_IF	interrupt on reception of a full command packet.
~IRQ2	MHC	interrupt on reception of byte on the UART.
~IRQ1	ROE	interrupt on reception of byte on the UART.
~IRQ0	MD_IF	interrupt on transmission of final word of sub-packet.

3.5 Boot Function FPGA - (Boot_Ctl)

In the EIS ICU a default set of program code, data, tables, and sequences are stored in non-volatile PROM's and EEPROM's.

In 48-bit long instructions are stored in the PROM in a serial byte format. At POWER-ON, or during a WARM_REBOOT, the Boot_Ctl FPGA holds the DSP in a RESET condition whilst reading six bytes at a time from the PROM starting at address **0x00 0000**. The six byte instruction formed can then be written to Program RAM from address **0x00 0000**. The next six bytes are read from PROM (which is from address **0x00 0005**) and written to Program RAM address **0x00 0001**. In this manner a very small "Boot-Loader" program is copied from PROM to RAM. Then the DSP RESET line is released and the DSP starts execution of the code copied to RAM.

3.6 MDP-ICU Interface Differential Driver Circuits

Details of the interface circuit requirements between the ICU and MDP are in AD2.

The EIS_ICU uses filter coils as recommend in document AD2.

3.7 Test Connectors

Two test connectors are provided on the SC_PROC board:

3.7.1 OD Test Port

A 40-way IDC header is provided for test debugging. This provides the un-buffered signals **PMD[47:16]**, **~WRM_RST, ~OD0, ~OD1, GND** and **VDD.** The two **~OD** signals are decoded ports. Software can write 32-bit data to these addresses. These signals go to a test circuit which buffers the data bus to a FIFO. The FIFO data is then transmitted to a PC via standard RS-232 UART interface. The **~WRM_RST** allows the test circuit FIFO's to be reset when ever the ICU is reset. **~OD0** is used to latch data bits **PMD[31:16]** on the test board; **~OD1** is used to latch data bits **PMD[47:32]** on the test board**.** These two signals can be linked together to provide a single strobe signal to the FIFO's.

3.7.2 JTAG Port

This port allows programs to be downloaded to memory, programs to be single-stepped, and DSP registers to be observed.

See CD-ROM for data sheet: \Solar-B\ICU Design Data Sheets\Processor\Temic21020f.pdf and Analog Devices ADSP-21020 User Manual.

4 PM_ICU Memory Map

4.1 Program Memory Space

Memory Bank		Physical Address	PMA[23,22,21]
Bank 0 (PMS0*)	Program RAM	0x00 0000 128k * 48-bit RAM 3 wait states 0x01 FFFF	000
Bank 1 (PMS1*)	Not Used	0x20 0000 0x7F FFFF	000
	CM_Ctl I/O Ports	0x80 0000 h/w & s/w defined wait states 0x8B FFFF	100
	Not Used	0x8C 0000 0x9F FFFF	100
	MON I/O Ports	0xA0 0000 3 wait states 0xA0 000F	101
	Not Used	0xA0 0010 0xBF FFFF	101
	SC_PROC I/O Ports	0xC0 0000 3 wait states 0xCF FFFF	110
	PROM	0xE0 0000 32k * 8-bit PROM 3 wait states 0xE0 7FFF	111

4.2 Data Memory Space

Memory Bank		Physical Address
Bank 0 (DMS0*)	Data RAM	0x0000 0000 128k * 32-bit RAM 3 wait states 0x0001 FFFF
Bank 1 (DMS1*)	CCD Buffer	0x0100 0000 2M * 16-bit RAM H/W wait states 0x011F FFFF NOTE: Buf_A & Buf _B occupy the same address space.
Bank 2 (DMS2*)	Working RAM	0x0200 0000 512k * 32-bit RAM 3 wait states 0x020F FFFF
Bank 3 (DMS3*)	EEPROM	0x0300 0000 1M * 8-bit EEPROM (8 off) H/W wait states 0x030F FFFF
	Not Used	0x0310 0000 0xFFFF FFFF (top of Data space)

4.3 PM_ICU I/O Port Map – Program Memory (Bank 1) - PMS1*

Base Address		Function: address(HEX)	Port Name	Note
PMA				
[23:21]	**[3:0]**	**Space Craft Time IF: 0xC0 0000**		32-bit counter
11x	**0000**	SCTIME Control Register	SCTIME_WR	Load new time value from Space Craft
	0000		SCTIME_RD	Read current time value
		Watchdog IF: 0xC0 0001		approx. 7/15sec time-out circuit
	0001	WATCHDOG Control Reg.	WATCHDOG_CTL_WR	Counter RESET, EN/DISABLE
	0001	Read WATCHDOG Status	WATCHDOG_STAT_RD	WatchDog trip status etc.
		Command IF: 0xC0 0002		
	0010	CMD Control Register	CMD_CTL_WR	Reset, Read from FIFO, interrupt etc
	0010	CMD Status Register	CMD_STAT_RD	Status information register
		Command IF: 0xC0 0003		
	0011	Read CMD Buffer Data	CMDDATA_RD	8-bit port from FIFO buffer
		Status IF: 0xC0 0004		
	0100	ST Control Register	ST_CTL_WR	Reset, Write to FIFO, etc
	0100	ST Status Register	ST_STAT_RD	Status information register
		Status IF: 0xC0 0005		
	0101	Write Data to ST Buffer	STDATA_WR	8-bit data port to FIFO buffer
		Mission Data IF: 0xC0 0006		
	0110	MD Control Register	MD_CTL_WR	Reset, Write to FIFO, etc
	0110	MD Status Register	MD_STAT_RD	Status information register
		Mission Data IF: 0xC0 0007		
	0111	Write Data to MD Buffer	MDDATA_WR	16-bit port to FIFO buffer
		Odmeter IF: 0xC0 0008		
	1000	Write Data to OD port #0	OD0_WR	Latch 32-bit value to HEX display
		Odmeter IF: 0xC0 0009		
	1001	Write Data to OD port #1	OD1_WR	Latch 32-bit value to HEX display
		Free Address:		
	1010			
	to	spare	spare	
	1111			
100	xxxx	**CM_Ctl: 0x80 000x**		
	see AD5	Camera/MHC Control Registers	see AD5	see AD5
	see AD5	High Speed Link Control Registers	see AD5	see AD5
101 see AD6	xxxx	**PSU Monitor IF: 0xA0 000x**		
	see AD6	PSU Monitor Control	see AD6	see AD6
		Free Address:		
	0010			
	to	spare	spare	
	1111			

PMA[20:4] = don't care.

5 Schematics

Drawing Number:

5275/009-5	Issue 1

Hierarchical list of sheets:

PM_ICU.1	Issue 1
SC_PROC.1	05/05/2001
SC_BUS.1	03/04/2001
DSP.1	28/03/2001
DAT_RAM.1	28/03/2001
PRG_RAM.1	28/03/2001
TWIB_CTL.1	03/05/2001
TTWIB_CTL.1	03/05/2001
ACTEL_45.1	28/05/2001

Mechanical Drawing:

SC_PROC Board Profile	A2/5275/009-5 Issue 1

6 Actel FPGA Programming Information

The design files for the FPGA are in the CD-ROM directory:

\Designs\Solar-B\PM_ICU.v2\Actels\Actel_45\

The part programmed is:

TWIB_CTL – A54SX32A-PQ208 – v1.2

signature: 000B3

user ID: b30

check sum: 8842

The device was programmed using the DOS version of Silicon Sculptor: DOS3.54 – 04/02/01 from laptop mssllkr-2

dev sum: 0086E2BFH

7 PCB Manufacturing and Board Assembly and Parts List

Drawing Number:

5275/009-5	assembly drawing and parts list	Issue 1 27/03/01
X-1639001	pcb	Issue 1 27/03/01

8 Bill of Materials

Generated from Viewlogic design for SC_PROC.1:

SC_PROC.LST	03/04/2001

Note: the part numbers show are for flight equivalent components (having footprints as for FM components).

9 Construction Operations

9.1 Links

Connect signals for unused gates to **GND**:

close: J4, J5, J6, J8, J9, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J23, J24

Connect signals '**OD0**' and '**OD1'** together:

close: J7

Connect signal '**COM**' to p.c.b. **GND** signal:

close: J2

For testing the PROM is replaced by an EEPROM. This device has a '**~WR**' signal which is connected to the DSP. For the FM_ICU this pin is pulled high – i.e. **J10 = open**:

close: J10

Connect Actel user signal '**CLKB_OUT**' output to Actel '**CLK_B**' input signal:

close: J11

9.2 Select on Test Items

none.

9.3 Modifications

IN PLACE OF	**FIT**
PROM U9: 28-way 0.3" socket 128k x 8 SRAM: U11-U20 UT7Q512-ICX: U21 – U24	28-way 0.6" to 0.3" converter socket ISSI part IS1C1024L (25ns) UT7Q512-UPC

- The pinout of the JTAG test connector, 'LK3' is incorrect. Do not fit header.
- For **U21-U24** note that the pinout for the UT7Q512-UPC is very different from the FM part. Use pinout diagrams in data sheet to rewire the part to the p.c.b.
- For SRAM's **U11-U24** the 'J' bend of the pins has to be straightened out from one side of the package to allow wires to be attached.
- Label **DMS[3:0]** on 'DSP' symbol bus and 'SC_BUS' symbol bus should be **~DMS[3:0]**- i.e. the "inverting" bar is missing from the signal name. Thus, signals **~DMS0** on **U17 – U20** ('DATA MEMORY SRAM'), and **~DMS2** on **U21 – U23** (Working SRAM) do not route to the DSP or backplane:

  ~DMS2: add wire link from R118/1 to U22/22

  ~DMS0: add wire link from R116/1 to X120

- Re-routing of interrupts '**~IRQ2**' and '**~IRQ1**':

  U1/MD_IRQ, test point – X123 to R100/2 – note R100/2 pin is taken out of its pad, and the wire soldered to the resistor

  U38/7 to U1/MHC_IRQI, test point - X124

- '**~DMS3_B**' & '**~DMS1_B**' from **U27** to Backplane are crossed over from the signal from the DSP:

  remove R93 and R95 and cross wire them.

- Add a RESET push-to-make switch during testing:

  wire across J3 and route to front panel

- For the Silicon Explorer test connector add:

  TCLK: 10k resistor from J1/4 to GND

  TDI: 10k resistor from J1/5 to GND

  TRSTB: 10k resistor from J1/7 to GND

  VCC: add wire from +5V source to a flying test lead. **WARNING**: add an insulating cover-cap to test lead to stop it shorting to any near by signals.

- On **U27** - DSP pin '**#159**' - '**EVDD'** signal is routed incorrectly to '**EGND**'. Do not solder this leg to the pad, and insulate it.

- Signals **~MD_DATAP** and **MD_DATAN** are labelled incorrectly from D-type25 connector **CN1** to filter core **F6**, and are cross routed:

  cut track from **CN1/4** to **F6/3** near core **F6**

  cut track from **CN1/5** to **F6/4** near core **F6**

  add wire from **CN1/4** to **F6/3**

  add wire from **CN1/5** to **F6/4**

- For signal termination on **~MD_WR** to FIFO:

  cut track between **DSP – U1** and FIFO **U5/1**

  solder 47R resistor across cut track

  add 22k pull-up resistor from **U5/1** to **VCC**

- For signal termination on **~MD_RD** to FIFO:

  cut track between **DSP – U1** and FIFO **U5/15**

  solder 47R resistor across cut track

- Connect screw-lock to 'OVERALL_SCN0':X10 or'OVERALL_SCN1':20

- additional de-coupling capacitors:

  add 22nF capacitors across **U26, U27, U29, U30, U33**

  add 10nF capacitors across **U26, U27, U29, U30, U33**

  add 22nF capacitors across **C30, C34, C38, C40, C70, C71**

10 Updated Schematic

none

11 Layout Instructions

11.1 Input to Mentor

Files are generated from a Viewlogic conversion utility to mentor format.

NO modifications allowed to COMPS_FILE OR NETS_FILE without permission from **RAC**.

Filename & path	Description
~\Designs\Solar-B\PM_ICU.v2*.*	Viewlogic PM_ICU SC_PROC design directory
~\Apps\WV7.53\STANDARD \mentor.cfg	Viewlogic netlister congifuration control file for Mentor system
~\Designs\Solar-B\PM_ICU.v2 \ men_SC_PROC\comps_file.cmps	Viewlogic component packages file
~\Designs\Solar-B\PM_ICU.v2 \ men_SC_PROC\nets_file.net	Viewlogic design netlist file

11.2 Notes

Take note of the orientation of components such as I.C.'s which do **NOT** all flow in one direction, and resistors: most resistors are vertically mounted, so it is important which pad is covered by the body, as the wire-end is used for test measurements.

11.3 Feedback from Mentor

nets.nets_1 => renamed to nets_file.lo1

comps.comps_22 => renamed to comps_file.lo1

12 Layout Changes

none.

13 Parts List

sc_proc Tuesday, April 3, 2001 2:22 pm

#	QTY	REFDES	DEVICE	VALUE	PKG_TYPE	PART_SPEC
1	1	C1	ELECTROLYTIC_CAP	0.1U25V	CSS13B	0.6"L(B) 0.4"L(A)
2	44	C2,C3,C4,C5,C8,C10, C11,C12,C14,C16, C17,C18,C19,C20, C22,C24,C42,C43, C44,C45,C46,C47, C50,C51,C52,C53, C55,C56,C57,C59, C60,C61,C62,C63, C68,C69,C70,C71, C72,C73,C74,C75, C76,C77	SM_CAPACITOR_1206	10NF	1206	SM_CAPACITOR_1206
3	31	C6,C7,C9,C13,C15, C21,C23,C25,C26, C28,C29,C30,C31, C32,C33,C34,C35, C36,C37,C38,C39, C40,C41,C48,C49, C54,C58,C64,C65, C66,C67	SM_CAPACITOR_1206	100NF	1206	SM_CAPACITOR_1206
4	1	C27	SM_CAPACITOR_1206	100PF	1206	SM_CAPACITOR_1206
5	1	CN1	DFRA25		DBM25S_1AON	D-TYPE 25-WAY R/A FEMALE
6	1	CN2	IDC_40M		IDC_40_S	
7	1	D1	1N4148	1N4148	DO35	1N4148 DIODE
8	6	F1,F2,F3,F4,F5,F6	CORE	10MM	CORE_TN10-6-4	FERRITE CORE FILTER
9	1	J1	CON8		HEADER_1X8WAY	HEADER 8-WAY 0.1 PITCH
10	23	J2,J3,J4,J5,J6,J7, J8,J9,J10,J11,J12, J13,J14,J15,J16, J17,J18,J19,J20, J21,J22,J23,J24	2-PIN_JUMPER		SIL2	0.1 PITCH LINK
11	2	L1,L2	FILTER	1UH	IM4	POWER LINE FILTER
12	2	LK1,LK2	HEADER4X2		HEADER_2X4WAY	2X4 BLOCK OF LINKS
13	1	LK3	HEADER6X2		HEADER_2X6WAY	2X6 BLOCK OF LINKS

#	QTY	REFDES	DEVICE	VALUE	PKG_TYPE	PART_SPEC
14	2	P0,P1			HPF098AMBK0020	HYPERTAC 98-WAY R/ANGLE MALE
15	20	R1,R2,R17,R18,R19, R20,R21,R23,R63, R166,R167,R168, R169,R170,R171, R217,R218,R219, R220,R221	RLR05_VERTICAL	100R	RLR05_V	RESISTOR_RLR05_VERTICAL
16	8	R3,R4,R5,R8,R9,R10, R11,R12	RLR05_VERTICAL	4K7	RLR05_V	RESISTOR_RLR05_VERTICAL
17	6	R6,R7,R13,R14,R15, R16	RLR05_VERTICAL	33R	RLR05_V	RESISTOR_RLR05_VERTICAL
18	65	R22,R68,R69,R70, R71,R72,R73,R74, R75,R76,R77,R82, R83,R84,R85,R86, R87,R88,R89,R90, R96,R97,R99,R102, R103,R165,R172, R173,R174,R175, R176,R179,R180, R182,R183,R184, R185,R186,R187, R188,R189,R190, R191,R192,R193, R194,R195,R196, R197,R198,R199, R200,R201,R202, R203,R204,R205, R206,R207,R208, R209,R210,R211, R212,R213	RLR05_VERTICAL	22K	RLR05_V	RESISTOR_RLR05_VERTICAL
19	1	R24	RLR05_VERTICAL	SOT_470K	RLR05_V	RESISTOR_RLR05_VERTICAL
20	1	R25	RLR05_VERTICAL	SOT_220K	RLR05_V	RESISTOR_RLR05_VERTICAL
21	119	R26,R27,R28,R29, R30,R31,R32,R33, R34,R35,R36,R37, R38,R39,R40,R41,	RLR05_VERTICAL	47R	RLR05_V	RESISTOR_RLR05_VERTICAL

#	QTY	REFDES	DEVICE	VALUE	PKG_TYPE	PART_SPEC
		R42,R43,R44,R45, R46,R47,R48,R49, R50,R51,R52,R53, R54,R55,R56,R57, R58,R59,R60,R61, R62,R64,R65,R66, R67,R78,R79,R80, R81,R91,R92,R93, R94,R95,R98,R100, R101,R104,R105, R106,R107,R108, R109,R110,R111, R112,R113,R114, R115,R116,R117, R118,R119,R121, R122,R123,R124, R125,R126,R127, R128,R129,R130, R131,R132,R133, R134,R135,R136, R137,R138,R139, R140,R141,R142, R143,R144,R145, R146,R147,R148, R149,R150,R151, R152,R153,R154, R155,R156,R157, R158,R159,R160, R161,R162,R163, R164,R177,R178, R181,R214,R215,R216				
22	1	R120	RLR05_VERTICAL	1K8	RLR05_V	RESISTOR_RLR05_VERTICAL
23	8	RS1,RS2,RS3,RS4, RS5,RS6,RS7,RS8	8_RESISTOR_SIL	22K	SIL9	8_RESISTOR_SIL
24	1	U1	ACTEL_45	WIB_CTL	CQPQ208_IN_SKT	A54SX32S_208_PINOUT
25	1	U2	HS26C32		DIP16	QUAD DIFFERENTIAL RECEIVER
26	6	U3,U4,U5,U6,U7,U8	IDT7204TP	4K_FIFO	DIP28_C	IDT 4K * 9 ASYNC FIFO-300MIL PKG

#	QTY	REFDES	DEVICE	VALUE	PKG_TYPE	PART_SPEC
27	1	U9	UT28F256	256K_PROM	DIP28	UTMC 256K PROM
28	1	U10	ACS32MS		DIP14	2 I/P OR GATE
29	10	U11,U12,U13,U14, U15,U16,U17,U18, U19,U20	LMFS1024_234	128K_SRAM	CFP32_0.65	LM 128K SRAM-32-PIN WIDE FP
30	4	U21,U22,U23,U24	UT7Q512-ICX	512K_RAM	CFP36_0.4	SHEILDED 512KX8-BIT UTMC SRAM
31	1	U25	TSC21020F	21020_DSP	MQFP256	TEMIC TSC21020F-20SB
32	10	U26,U27,U28,U29, U30,U31,U32,U33, U34,U35	54AC245		DIP20	OCTAL TRI-STATE TRANSCEIVER
33	2	U36,U37	HS26C31		DIP16	QUAD DIFFERENTIAL DRIVER
34	2	U38,U39	54AC244		DIP20	OCTAL TRI-STATE BUF
35	1	U40	54AC08		DIP14	2 I/P AND GATE
36	1	U41	54HC14		DIP14	SCHMITT HEX INVERTER
37	48	X1,X2,X3,X4,X5,X6, X7,X8,X9,X10,X11, X12,X13,X14,X15, X16,X17,X18,X19, X20,X21,X22,X23, X24,X25,X26,X27, X28,X29,X30,X115, X116,X117,X118, X119,X120,X121, X122,X123,X124, X125,X126,X127, X128,X129,X130, X131,X132	TEST_POINT		C063_PAD	TEST POINT
38	1	XT1		20MHZ	IQXO-22	LOW PROFILE/HC18U FOOTPRINT

	436					