Solar B – EIS

MULLARD SPACE SCIENCE LABORATORY

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PM ICU HARDWARE DESIGN DEFINITION

Document Number: MSSL/SLB-EIS/DD010.01

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CHANGE RECORD

ISSUE	DATE	PAGES CHANGED	COMMENTS
01	29 October 2001	All new	

Machine File-System Directory:	\\msslk6\d:\Solar-B\Documents\ICU_Design\PM_ICU Model
Document File Name:	PM_ICU_DesignDD10-01.doc
Application:	MS Word 2000
Included files:	
Print Date (this):	29-Oct-01 @ 16:03
Printer:	Postscript

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1 Introduction

The Solar-B Instrument Control Unit (ICU) comprises the ICU-crate and six boards:

1) PSU0: Power Supply Unit board #1
2) MON: Monitor card
3) CM_CTL: Camera/MHC Control card
4) SC_PROC: space craft interfaces and processor card
5) PSU1: Power Supply Unit board #2
6) PM_Bkpl: PM ICU Backplane

The SC_PROC, and CM_CTL make up the main digital processing and interfacing electronics. The MONITOR and PSU cards provide power supply conditioning, switching and power and health monitoring functions.

2 SCOPE

The PSU cards are being designed as a separate block, and as such details of this card may be found in document: AD5.

This document describes the top level design of the prototype model of the ICU (PM_ICU) consisting of:

1) SC_PROC
2) CM_CTL
3) MON
4) PM_ICU Backplane

More detailed information about the individual cards or ICU-crate can be found in the relevant document as referenced below.

3 APPLICABLE DOCUMENTS

AD1: MSSL/SLB-EIS/SP003 Interface Control Document
AD2: MSSL/SLB-EIS/DD012 PM ICU Processor Board Design Definition
AD3: MSSL/SLB-EIS/DD019 PM ICU Camera/MHC Control Board Design Definition
AD4: MSSL/SLB-EIS/DD018 PM ICU Monitor Board Design Definition
AD5: MSSL/SLB-EIS/DD017 PM ICU Power Board Design Definition
AD6: MSSL/SLB-EIS/DD011 PM ICU Backplane Design Definition
AD7: MSSL/SLB-EIS/SP004 Mass Budget
AD8: MSSL/SLB-EIS/CF001 Configuration Item Data List for the PM
AD9: Drawing #5275-303 Mechanical drawings for PM_ICU crate

4 ICU Digital Electronics

Figure 1 shows a diagram of the PM ICU electronics. The main requirement of the PM_ICU is to have a flight representative interface to the space craft. This includes the Command Interface (CMD_IF), Status Interface (ST_IF), Mission Data Interface (MD_IF), and the Main Power & Control Interface.

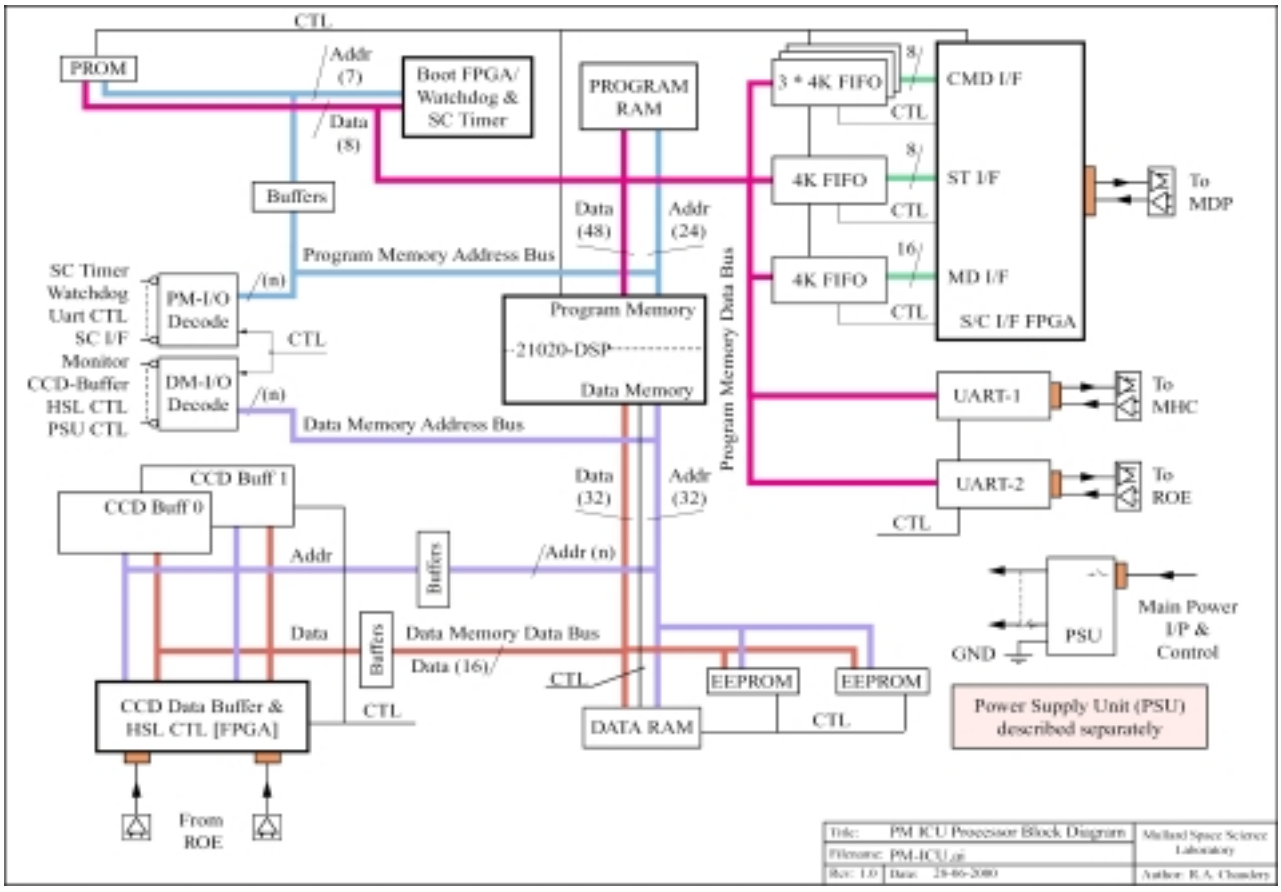

Figure 1 PM_ICU Block Diagram

Figure 2 is a block diagram showing how the electronics is partitioned across the three main circuit boards.

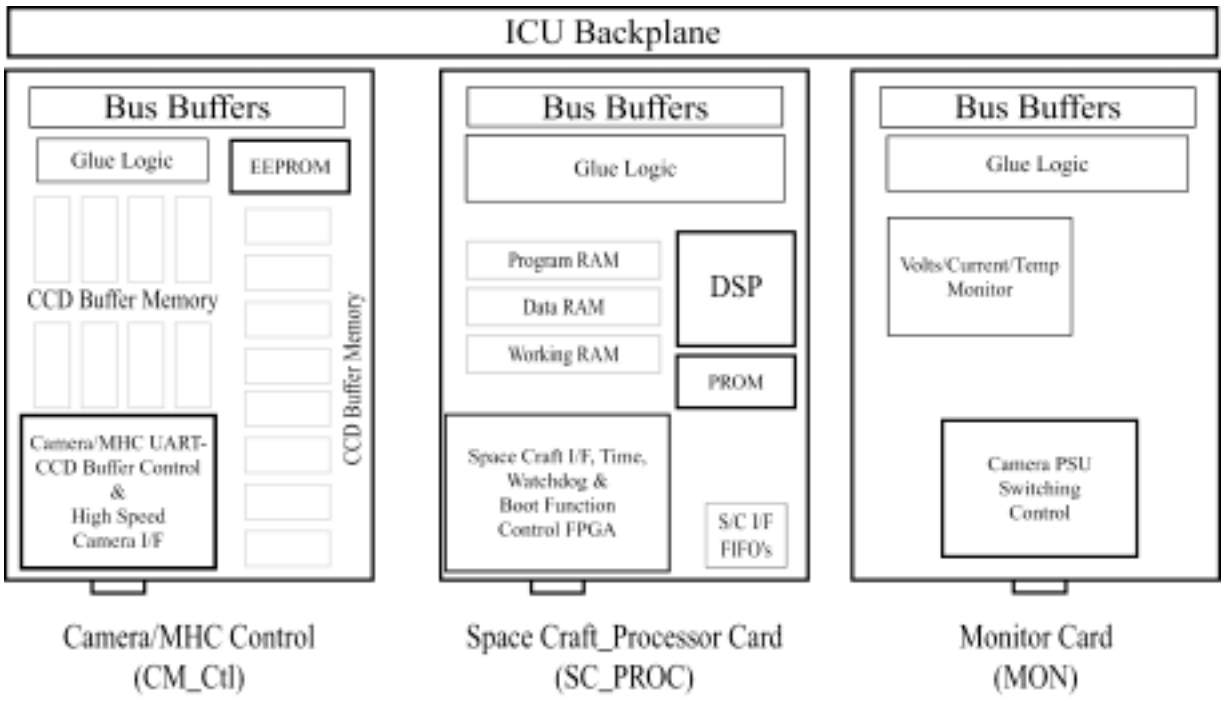

Figure 2 PM_ICU Block Diagram

The PM ICU differs from the FM design as follows:

- the use of commercial or engineering components.
- some parts, such as the 512k * 8-bit SRAM memory, EEPROM, 128k * 8-bit SRAM memory have different package pin outs and outlines
- the PSU card does not meet any EMC or in-rush current specification.
- the MON card does not provide any voltage, current or temperature monitors.
- the p.c.b. layout of the CM_CTL, MON and PSU cards is not the same for FM design.

4.1 ICU Prototype Model Overview

4.1.1 Space Craft Interface & Processor Card (SC_PROC)

The main components on this card are:

- 21020 DSP
- Program, Data and Working SRAM memory
- Boot PROM
- interface FIFO's
- Actel FPGA with all interfaces, watchdog, space-craft time and decoding circuitry
- Address, data, and control line buffers to the Backplane.
- Differential drivers for the space craft interfaces.

See Ad2 for the detailed design of the SC_PROC card.

4.1.1.1 DSP Processor

The Processor used for the ICU design is the TSC21020F running at 20MHz. This is based on the Analog Devices 21020 DSP core. For the PM ICU design an engineering version of the processor is used, housed in a 256 pin ceramic quad flat pack (CQFP).

This DSP uses a Harvard architecture: there are two separate processor buses labelled as PROGRAM MEMORY and DATA MEMORY. Each side has a complete set of control signals allowing the processor to effectively read or write to both memory areas simultaneously.

The program memory interface is 48-bit wide, which is the instruction width, allowing several parallel operations to be executed. The program memory area can directly address up to 16M * 48-bit words using four PROGRAM MEMORY decode signals. These decodes are user selectable in software.

The data memory interface is 40-bit wide. The data memory area can directly address up to 4G * 40-bit words using four DATA MEMORY decode signals. These decodes are user selectable in software.

There is a JTAG test port available on the DSP which can be used during development for debugging software or hardware in semi real-time and also to download code to program or data SRAM areas. This functionality may not be available on the FM ICU as the JTAG port connector may not be accessible when the ICU is in its flight housing.

See Analog Devices ADSP-21020 User's Manual and the TEMIC 21020F Data Sheet for full details.

4.1.1.2 Program Memory

This is where program instruction code will be stored. This is mapped to the DSP as 128k by 48-bit SRAM in program memory address space. The processor may be run with zero wait state PROGRAM MEMORY accesses.

4.1.1.3 Data Memory

This is where variables, stacks, heaps and tables will be stored. This is mapped to the DSP as 128k by 32-bit SRAM in data memory address space. The processor may be run with zero wait state DATA MEMORY accesses.

4.1.1.4 Working Memory

This area will be used to buffer CCD mission data packets before transmission to the MDP. It will also be used for intermediate data manipulation.

The part used is the UTMC 512k by 8-bit UT7Q512-UPC I.C. with 100ns access speed.

This is mapped to the DSP as 512kbyte * 32-bit SRAM in data memory address space. The working memory requires three wait states for access control.

4.1.1.5 Boot PROM

A “Boot-Loader” circuit is implemented in a FPGA which holds the processor buses and control signals in a tri-state condition during the POWER-ON RESET cycle. During the reset period the Boot-Code BYTES (held in PROM) are shifted into a 48-bit wide “instruction register” inside the FPGA, and then written Program RAM. It is estimated that the maximum size of Boot-Code shall be less than 16kbytes.

4.1.1.6 Interface FIFO’s

The FIFO’s are 4k * 9-bit and provide buffers for CMD_IF, ST_IF and MD_IF data packets.

Because of the low SEU threshold of FIFO’s, the CMD_IF uses three FIFO’s connected in parallel so that a software voting scheme may be used to effectively raise the SEU threshold. There is no need for such a scheme for the MD_IF or ST_IF interfaces as the data held in these FIFO’s is less critical than that in the CMD_IF FIFO’s.

4.1.1.7 Actel FPGA

An A54SX32A Actel is used for the following functions:

- ICU BOOT controller function
- Space Craft Interfaces:
    - 8-bit COMMAND interface (CMD_IF)
    - 8-bit STATUS interface (ST_IF)
    - 16-bit MISSION DATA interface (MD_IF)
    - WATCHDOG function
    - SPACE CRAFT timer function
    - ICU memory map decoding

4.1.2 Camera/MHC Control Card (CM_Ctl)

The main functional blocks of this card are:

- The CCD image Double Buffer memory.

- Up to 8 byte-wide EEPROM's provide a default set of observing tables/sequences, and operational code.
- An A54SX32A Actel FPGA is used to implement the following functions:
    - There are two UART interfaces, used to control the camera and mechanisms with RS-422 specification drivers.
    - The High Speed Link (HSL) interface from the camera electronics to the ICU.
    - LVDS drivers.
    - The CCD Double Buffer controller. The four CCD read-out ports are mapped to four blocks of CCD data buffer memory.
    - DSP memory/control interfacing.

See AD3 for further details.

4.1.2.1 CCD Double Buffer Memory

There are two memory banks mapped to the same DSP DATA MEMORY space as 1M * 16-bit SRAM. However, at any point in time only one of the banks will actually be enabled for accesses from the DSP; the other bank will be switched for accesses from the High-Speed Link controller.

These banks are termed the 'Double Buffer'. Each bank of the double-buffer shall be capable of holding a single, full CCD image, i.e. 2048 * 512 * 16-bit = 1M * 16-bit.

After every exposure sequence the Double Buffer shall be toggled to connect from PROCESSOR to CAMERA source.

4.1.2.2 EEPROM

These are mapped to DATA MEMORY holding operational code, and a default Exposure-Set-up-Table. Access to EEPROM is controlled through the FPGA on the CM_Ctl board.

There are 8 * 128k * 8-bit EEPROM's implemented on the CM_Ctl board. These are standard 32-pin LCC packages. The requirements are for 6 EEPROM's (equal to the PROGRAM SRAM memory), but for the FM_ICU two multi-chip-module (MCM) EEPROM's shall be used, which have 4 * 128k * 8-bit EEPROM dies in a single unit. This vastly reduces physical space required.

There is a WRITE operations life-cycle issue associated with EEPROM's, so for FM write/update operations need to be controlled.

4.1.3 Monitor Card (MON)

The main functional blocks of this card are:

- TBD number of analogue voltage, current and temperature signals that are multiplexed to an TBD bit ADC.
- Main Power Input and switching control.
- Camera power supply lines and control.

See AD4 for further details.

4.1.4 PM_ICU Backplane (PM_Bkpl)

The Backplane is designed to minimise transmission line problems associated with fast clocking frequencies, and so board positions are laid out to minimise track lengths. Also, analogue and power signals are kept separate from the digital signals as much as possible.

The five boards are laid out in the following order:

Board #	Label	
4	PSU1:	Power Supply Unit board #2
3	SC_PROC:	space craft interfaces and processor card
2	CM_CTL:	Camera/MHC Control card
1	MON:	Monitor card
0	PSU0:	Power Supply Unit board #1

Board #0 is the bottom board in the crate: board #4 is the top board.

The main digital signal flow is between the SC_PROC board and the CM_Ctl board. The MON board has the main signal flow from the PSU0 board, and some interface signals from the SC_PROC board.

Board #4 – PSU1 shall be used if the PSU design does not fit onto PSU0. Note that it is board #4 that occupies the “cut-out” section in the ICU crate structure. This is the reason that the main SC_PROC or CM_Ctl boards ca not be placed to one end of the crate – which would have kept them completely separate from the PSU and MON boards.