SWIFT UVOT Detector Safety Circuit Specification

MSSL/SWT-UVOT/SP/006.01

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1. Introduction

The information in this specification is drawn from the documents shown below and discussions and e-mail correspondence with Tom Kennedy and Hajime Kowakami and Phil Thomas.

> SWIFT UVOT Bright Source safety Philosophy Issue 1
> Blue detector processing electronics detailed design XMM-OM/MSSL/SP/0056.03

2. Top Level Requirements

1. Protect detector system against bright sources
2. Immune to false triggers due to penetrating radiation in the detector system
3. Fast reaction time to prevent damage to detector system
4. Fit within existing UVOT TM electronics architecture
5. Must not affect system performance
6. Must be controlled by ICU
7. Flexibility to cope with changing circumstances
8. Monitor detector count rates
9. Must be able to be calibrated inflight
10. Must be able to be TURNED OFF

3. Operational Philosophy

1. Use characteristics of optics to detect bright sources, the brighter the source the greater flair is observed
2. Use raw CCD output to detect consecutive pixels above a preset threshold
3. Count pixels above a preset threshold
4. Alert on multiple consecutive frames with consecutive pixels to counter false triggers due to penetrating radiation
5. Safe detector system by setting cathode voltage to 0V (this gives a detector gain reduction of ~10,000)

4. Safety Circuit Description

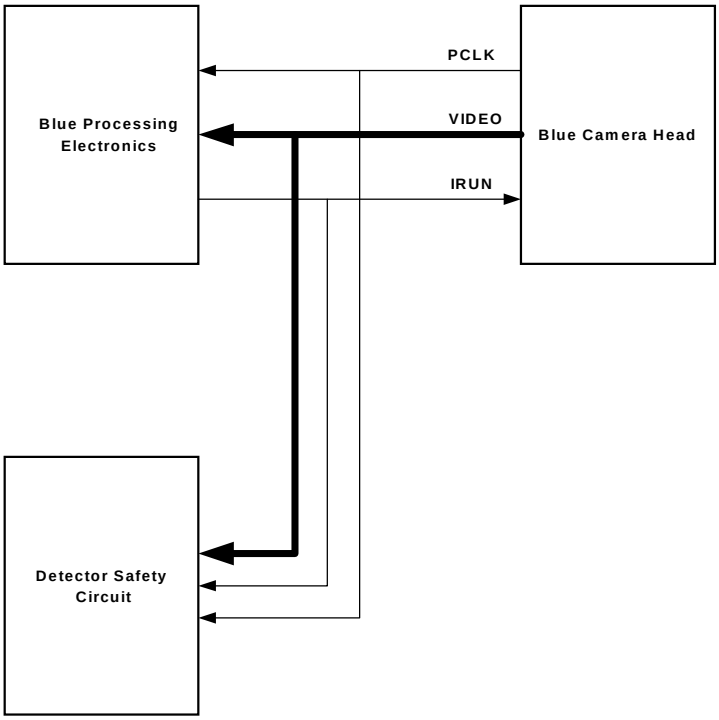
The purpose of the Detector safety circuit is to protect the UVOT detector system against damage from prolonged exposure to bright sources. This is achieved by two methods:

1. monitoring the number of pixels above a preset threshold for a fixed integration period. This counter will be accessable by the ICU via the ICB.

2. Detecting a preset number of consecutive frames with a preset number of consecutive pixels above a preset threshold.

Only valid pixels are counted by the safety circuit, the ~IRUN signal is used to detect the start of a frame and ~HRUN signal is used to determine when valid data is clocked out of the CCD by the horizontal clock. Data from the DUMP period is not counted by the safety circuit. This is achieved by ignoring the first ~HRUN period following a new frame.

The safety circuit is designed to deal with single full frame windows, if small or multiple windows are selected, the safety circuit will not function as required.



The UVOT safety circuit consists of three parts:

- The detector rate monitor
- Saturated pixel detector
- BPE interface

The most significant 5bits of video are used in the safety circuit, the 3 LS bit are treated as don't care.
The detector rate monitor and saturated pixel detector count only valid pixels. CCD dump phase after frame transfer is ignored and subsequent video data is enabled by the ~HRUN signal.

4.1 The Detector Rate Monitor

The rate monitor counts the number of above threshold pixels in a predetermined time period. The rate monitor is asynchronously sampled by the ICU via the MACS bus interface. The value read is the value from the previous sample period. The counter is sized to 24bits to overcome the problem of rollover at high-count rates. The value read back from the MACS bus is reduced to 23 bits to simplify bit packing in the read register. The means that the data bits transmitted are [23:1] this has the effect of dividing the output value by 2. The ICU should compensate for this.
In order to avoid incorrect values by sampling during the counter update period the ICU should sample at least 3 times (within a few hundred micro seconds) and only accept a value which occurs twice during the sample period.

Specification

	Fixed integration time	0.7 seconds	63 frame periods
Input	Input pixel threshold	5 bits	
Output (read back)	Input threshold	5 bits	
	counter	24 bits	From previous integration period
		23bits	read register

4.2 The Saturated Pixel Detector

The saturated pixel detector counts the number of consecutive pixels above a threshold, and if these events occur for more than a predetermined number of frames then the alert output activates. Writing to the control register controls the detector. The control functions are; alert reset, system enable and alert enable, see register allocation for more detail.

Specification

Input	Input threshold	5bits	Most significant
	Consecutive pixels	7bits	
	Consecutive frames	5bits	
	Alert reset	1 bit	
	System enable	1 bit	
	Alert enable	1 bit	
	Frame sync	1	~IRUN
	Horizontal read out control	1	~HRUN
Output (read back)	Input threshold	5bits	
	Consecutive pixel preset	7bits	
	Consecutive frame preset	5bits	
	System reset	1 bit	
	Alert reset	1 bit	

	Alert flag output	1 bit	
	System enable	1 bit	
	Alert enable	1 bit	
Output	Cathode safe signal	1 channel	link to monitor board

Control Signal Summary

System enable
This function enables both rate monitor and the saturated pixel detector. When asserted the command is internally synchronised to the next ~IRUN signal, allowing the system to start predictably.
Alert flag
This read register signal indicates that the SPD has fired, the cathode safe signal is asserted if the alert enable bit is set.
Alert reset
This function resets the cathode safe signal register to its powerup default state “off” (allowing control of the cathode voltage) and the alert flag would return a zero . The SPD circuit is also reset to its powerup default state. Control register functions are not affected by this signal, any previous state will be maintained until being rewritten or reset by power cycling.
Alert enable
This function enables the cathode safe signal register. The alert flag is not affected by this control. This allows for on orbit calibration of the system.

Typical operational sequence (after power up)
Set up SPD and ratemeter pixel thresholds (register 2)
Setup consecutive pixel and frame counts (register 1)
Read back and verify
Set system enable and alert enable bits.
Read back and verify
Powerup detector
Read ratemeter at regular intervals
Read alertflag bit at regular intervals
If alert flag =1

4.3 ICB Interface

The ICB interface uses the decoded MACS parallel bus from the BPE camera board. Two read and two write strobes are available. The implementation is shown below.
Read registers alternate between two possible sources, the source is identified by the REGID bit.

Memory Map

Read Addresses

ICB address	Sub address	Function
0x18	0x0	Read register 1
	0x1	Read register 2

Write Addresses

ICB address	Sub address	Function
0x18	0x0	Write register 1
	0x1	Write register 2

Detector Safety Circuit Register allocation

WRITE register 1 ICB sub address 0x0		
B15	N/A	Not assigned
B14-B8	PCTHOLD[6:0]	Consecutive pixel count
B7	OPRST	Output reset 1=reset
B6	SYSEN	System enable 1=enable
B5	ALERTEN	Cathode control 1=enable
B4-B0	FCTHOLD[4:0]	Consecutive frame count

WRITE register 2 ICB sub address 0x1		
B12-B8	STHOLD[4:0]	Pixel threshold
B4-B0	RTHOLD[4:0]	Ratemeter pixel threshold

READ register 1 ICB sub address 0x0		
REGID=0		
B15	REGID	Register identification bit
B14-B8	RATE[15:9]	Rate meter output
B7-B0	RATE[8:1]	Rate meter output

READ register 1 ICB sub address 0x0		
REGID=1		
B15	REGID	Register identification bit
B14-13	N/A	Not assigned
B12-B8	RTHOLD[4:0]	Ratemeter pixel threshold
B7-B0	RATE[23:16]	Rate meter output

READ register 2 ICB address 0x1		
REGID=0		
B15	REGID	Register identification bit
B14-B8	PCTHOLD[6:0]	Consecutive pixel count

B7-B5	N/A	Not assigned
B4-B0	STHOLD[4:0]	Pixel threshold

READ register 2 ICB address 0x1		
REGID=1		
B15	REGID	Register identification bit
B14	ALERTFLAG	Alert output register
B13	OPRST	Safety circuit reset
B12	ALERTEN	Enables cathode control
B11	SYSEN	Enables safety circuit
B10-B5	N/A	Not assigned
B4-B0	FCTHOLD[4:0]	Consecutive frame count

4.4 Cathode Safe Signal

The safety circuit can power down the cathode of the detector via a direct connection on the BPE motherboard to the monitor card. The output is reset when the OPRST bit is set to 1 and returned to 0 when operation is to continue.