SWIFT TMPSU MACS/control system. Memory Map And Operational Description. JAT 18/12/01

Note:-

The TMPSU MACS address will be set up as 0X07 by default, same as OM.

Only data bits 0-7 (msb 8 bits) are used in write commands.

The address is only decoded for writes and only the bottom three bits are used in the decoding (so the decoding is repeated four times).

A read from any address will select the same parameters.

Write Addresses.

Address 0. HK Channel Select and FW LED drive. Latch is cleared on power up.

Bit	Name	Description.
0 MSB	CHS0	MSB of HK channel select.
1	CHS1	
2	CHS2	LSB of HK channel select. See below for sub address selection.
3	FW_PSC0	MSB of LED current set up.
4	FW_PSC1	
5	FW_PSC2	
6	FW_PSC3	LSB of LED current set up. See below for count to current conversion.
7	Spare.	

HK Channel Select		Calibration where x is the adc count in decimal		
CHS	Description.	QM	FM-1 (SFT02)	FM-2 (SFT03)
0	+28V current	= 0.0042x + 0.0044 A	= 0.0040x - 0.0023 A	= 0.0041x +0.0075 A
1	+11V current	= 0.0020x - 0.0221 A	= 0.0020x - 0.0001 A	= 0.0020x + 0.0161 A
2	+15V current	= 0.0012x - 0.0200 A	= 0.0012x + 0.0025 A	= 0.0012x + 0.0080 A
3	-15V current	= 0.0012x - 0.0215 A	= 0.0012x - 0.0071 A	= 0.0012x - 0.0013 A
4	+5VB current	= 0.0056x - 0.0430 A	= 0.0057x - 0.0148 A	= 0.0057x - 0.0233 A
5	+5VA current	= 0.0049x - 0.0093 A	= 0.0051x + 0.0057 A	= 0.0050x - 0.0069 A
6	-5VA current	= 0.0033x + 0.0123 A	= 0.0035x + 0.0123 A	= 0.0036x + 0.0047 A
7	DISMON	= 0.0196x V	= 0.0196x V	= 0.0196x V

DISMON	QM	FM-1	FM-2
Off	0	0	0
FW	62	63	62
DM	112	114	114
Both	132	135	134 (TBC)

The monitoring of DISMON should allow for a few bits jitter, a count of +/-5 should suffice.

LED current.

FW_PSC	Current/mA	FW_PSC	Current/mA
0	0.01	8	58.8
1	7.35	9	66.2
2	14.67	10	73.5
3	22.01	11	80.9
4	29.36	12	88.2
5	36.7	13	95.5
6	44	14	102.9
7	51.4	15	110.2

Address 1. ADC Convert.

Any write to this address will start a conversion of the HK parameter set up in the previous address. The data value is Don't Care. The timing of the collection of HK is described below.

Address 2. Filter Wheel and Dichroic Mirror motor control. Latch is cleared on reset and by a motor ballast resistor warming up too much above ambient.

Bit	Name	Description.
0 MSB	FW_C0	Filter Wheel winding 0. A logic one energizes the winding.
1	FW_C1	
2	FW_C2	
3	FW_C3	
4	DM_C0	Dichroic Mirror winding 0. A logic one energizes the winding.
5	DM_C1	
6	DM_C2	
7	DM_C3	

Address 3. Temperature Control. Latch is set to a logic 1 on power up.

Bit	Name	Description.
0 MSB	Enable	When writing a logic 1, the circuit is enabled.
		When writing a logic 0, the circuit is disabled.
1-7	Not Used.	

Address 4. Heater Control. Write Only. Latch is cleared on power up.

Bit	Name	Description.
0	HTR_C0	Heater circuit 0. A logic one turns on the heater.
1	HTR_C1	
2	HTR_C2	
3	HTR_C3	
4-7	Spare.	

Address 5-7. Not Used.

Address 8-31. Repeat of the above.

Read Operation. From any address 0-31

Bit	Name	Description.
0	CV0	MSB bit of ADC value
1	CV1	
2	CV2	
3	CV3	
4	CV4	
5	CV5	
6	CV6	
7	CV7	LSB bit of ADC value
8-13	Not Used, always logic 1.	
14	ENABLE	Reflects status of Temperature control. A logic 1 means it is on, default on power up. A logic 0 means it is off.
15	FW_PSV	Filter wheel position sensor. A logic 1 means the reference point has been reached. A logic 0 means the reference point has not been reached.

Timing for the Multiplexer and ADC.

The time constant on the input to the ADC is 2mS (10K+10K ohms and 100nF) except for the DISMON channel (220K + 10K or 100K + 10K or 220K in parallel with 100K + 10K.). Therefore the time between selecting the analogue channel and telling the ADC to convert should be greater than or equal to 20mS except for DISMON. For DISMON the original OM timing of 100mS is to be used.

The ADC data sheet gives a maximum conversion time of 40uS. Some overhead should be given for the interfacing logic between the MACS chip and ADC, in the order of 5uS. Therefore the time between telling the ADC to convert and reading back the ADC data should be greater than 45uS (0.000045seconds)