2. Using appropriate holes and tracking made available in step 1 add inductor and capacitors as per sheet 2 of schematic.
3. Fit SOT 200 R resister to between hypertac pin 95 and PCLK signal. This sot will then be replaced with appropriate fixed value resister.

6. Layout Instructions

Use 50 thou tracks from hypertac +5V pins to current limit transistors. Net VBPE.

6.1 Input to Mentor

Files are generated from a Viewlogic conversion utility to mentor format.

6.2 Notes

6.3 Feedback from Mentor

The final netslist files after completion of the layout should be saved here:

ftp://128.40.70.7/Public/Mentor/BPE/PROCESS as "EM_Mentor_Net" and "EM_Mentor_Comp"

Machine File-System Directory:	\\MSSLi7\data\projects\XMM-OM/MSSL/DD/0023.01
Document File Name:	PROCESS.DOC
Application:	MS Word 6
Included files:	
Print Date (this):	22-Oct-97 @ 12:23
Printer:	Postscript

1. Schematics

Drawing Number: 5229/029 4-10-1997 Issue 3

Hierarchical list of sheets:

PROCESS 1

PROCESS 2

PROCESS 3

PROCESS 4

PROCESS 5

PROCESS 6

PROCESS 7

PROCESS 8

PROCESS 9

PROCESS 10

2. PCB Manufacturing and Board Assembly

Drawing Number: 5229/029-5 21-10-96 drill plot

5229/029-6 21-10-96 assembly drawing and parts list

Artwork: 1542-002

Serial Number:

Hypertac Position: C3

Fit all wire links

3. Bill of Materials

Database printout for BPE-PROCESS 20-10-97

4. QM Assembly List

QM assembly list can be found on assembly drawing see above.

5. Modifications

1. Do not fit T1, T2, R1, R2

MM Optical Monitor

MULLARD SPACE SCIENCE LABORATORY
UNIVERSITY COLLEGE LONDON Author: Duncan Self

MSSL *XMM*OM QM BPE PROCESS Design Definition

DOCUMENT: XMM-OM/MSSL/DD/0023.01

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