XMM Optical Monitor

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MSSL ^{XMM}OM ICU-DPU Backplane Connections

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Document Record

Issue	Date	Changes
01	15-Jan-96	New
02	14-Feb-96	
03	this	pins 33 and 34 on backplane - name correction

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1. Power lines.

From XMM-OM/MSSL/SP/0007 Section 3.1.3 “DEM Secondary Power”

VDR = VDR_ICU (In XMM-OM/PENN/SP/0008.01= VICUKAL)

VDBU

VICU

ResLatch†

† defined in XMM-OM/PENN/SP/0008.01 § 2.2.2 Note 2.

2. Time interface

From XMM-OM/MSSL/SP/0007 Section 3.2.3 “Time”

zerot = Time_ZeroT

tclk = Time_TClk

Note: Timing of t2 and t3 has been corrected such that ZeroT is high for one cycle of tclk.

3. SSI Interface

From XMM-OM/MSSL/SP/0007 Section 3.2.2 “SSI”

FTX = SSI_FTX (was FST)‡

FRX = SSI_FRX (was FSR)

DTX = SSI_RTX (was Tx)

DRX = SSI_DRX (was Rx)

CLK = SSI_CLK (was Clk)

‡ Updated in Issue 6 of XMM-OM/MSSL/SP/0007 to reflect backplane names.

4. Analogue Monitors

The following table relates the Backplane pinout to the document XMM-OM/PENN/SP/0008.01 § 3.0

Backplane Name	Reference	Description
MONA	3.2, current monitor for 2.1.2	IDPU measures VDPU supply
MONB	3.2, current monitor for 2.1.3	IICU measures VICU supply
MONC	3.2, sum current for 2.1.1 - 2.1.5	ISUM measures all supplies
MOND	3.1, voltage monitor for 2.1.2	measures VDPU supply
MONE	3.1, voltage monitor for 2.1.5	measures VDR_ICU supply

a simpler scheme may be considered:

MONA = IDPU+IICU (near the “+5.3V RECT & FILTER” block (PWR-81 Block Diagram @ 3B)

MONB = IKAL (near the “KAL 3.3V REG” block (PWR-82 Block Diagram @ 5B)

MONC = IDBU (in-line of “+9V” rail (PSU-10 XMM Power Supply Unit @ 4D)

and remove MONE

5. Backplane Issue 4.2

Bus	OMIF	EXP	MEM	SIBA	PROC			PROC	SIBA	MEM	EXP	OMIF	Bus
VICU	-	-	-	-	-	1	74	-	-	-	-	-	clk
as	-	-	-	-	-	2	73	-	-	-	-	-	resetn
dsn	-	-	-	-	-	3	72	-	-	-	-	-	rdyn
rdn	-	-	-	-	-	4	71	-	-	-	-	-	wrn
eas	-	-	-	-	-	5	70	-	-	-	-	-	gnd
rdwn	-	-	-	-	-	6	69	-	-	-	-	-	oin
mion	-	-	-	-	-	7	68	-	-	-	-	-	a8
a0	(expclk0)	(expclk0)	-	-	-	8	67	-	-	-	-	-	a9
a1	(expclk1)	(expclk1)	-	-	-	9	66	-	-	-	-	-	a10
a2	(spare0)	(spare0)	-	-	-	10	65	-	-	-	-	-	a11
a3	(spare1)	(spare1)	-	-	-	11	64	-	-	-	-	-	a12
a4	-	-	-	-	-	12	63	-	-	-	-	-	a13
a5	-	-	-	-	-	13	62	-	-	-	-	-	a14
a6	-	-	-	-	-	14	61	-	-	-	-	(RESLATCH)	a15
a7	-	-	-	-	-	15	60	-	-	-	-	-	d8
d0	-	-	-	-	-	16	59	-	-	-	-	-	d9
d1	-	-	-	-	-	17	58	-	-	-	-	-	d10
d2	-	-	-	-	-	18	57	-	-	-	-	-	d11
d3	-	-	-	-	-	19							
d4	-	-	-	-	-	20	56	-	-	-	-	-	d12
d5	-	-	-	-	-	21	55	-	-	-	-	-	d13
d6	-	-	-	-	-	22	54	-	-	-	-	-	d14
d7	-	-	-	-	-	23	53	-	-	-	-	-	d15
discon	-	-	-	-	-	24	52				adcrdwd	adcrdwd	
gnd	-	-	-	-	-	25	51	-	-	-	-	-	mproen
suren	-	-	-	-	-	26	50		zerot				
pwrok	-	-	-	-	-	27	49	rbiclk	rbiclk		adcrdst	adcrdst	
	ifinta	ifinta			ifinta	28	48		tclk		ifclk	ifclk	
	icbwrst	icbwrst			ifclk	29	47	prgrntn	prgrntn		SSICLK	MONA	
	ifintb	ifintb		resetmcn	resetmcn	30	46	as0	as0	as0	FTX	MONB	
	iodecn	iodecn		iodecn	ifintb	31	45	as1	as1	as1	FRX	MONC	
	icbwrcmd	icbwrcmd		bcp4intn	bcp4intn	32	44	as2	as2	as2	DTX	MOND	
	icbwrwd	icbwrwd		rbiintn	rbiintn	33	43	as3	as3	as3	DRX	MONE	
	icbwrxx	icbwrxx				34	42				icbrdxx	icbrdxx	
	adcwrst	adcwrst		dmae	dmae	35	41				icbrdwd	icbrdwd	
	adcwrwd	adcwrwd		prlckn	prlckn	36	40		VDBU		icbrdcmd	icbrdcmd	
	iordyn	iordyn	VDRicu	iordyn		37	39		VDBU		icbrdst	icbrdst	
VICU	-	-	-	-	-	38							
Note: pins marked - are bussed across all connectors													
signals in brackets (…) are in place of bussed signals													