XMM Optical Monitor

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MSSL ^{XMM}OM CCD Procurement Specification

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1. Scope

This document contains the requirements for the supply of 5 science and space flight grade imaging Charge Coupled Devices within 6 months from the placement of an order.

2. Reference Documents

[**1**] ASTM F 672-88, Spreading resistance in epitaxial layers.
[**2**] ESA/SCC 20490, Internal Visual Inspection of Integrated Circuits
[**3**] ESA/SCC 20500 External Visual Inspection
[**4**] ESA/SCC 21400. Scanning Electron Microscope Inspection Procedures
[**5**] MIL-STD-883, Test Method 1008, Test Condition D
[**6**] MIL-STD-883, Test Method 1010, Test Condition B
[**7**] MIL-STD-883, Test Method 2001, Test Condition A
[**8**] MIL-STD-883, Test Method 2002, Test Condition B
[**9**] MIL-STD-883, Test Method 2007, Test Condition A
[**10**] MIL-STD-883, Test Method 2011, Test Condition D
[**11**] MIL-STD-883, Test Method 2023, Test Condition D
[**12**] NAS 3447 Contamination Barrier for Precision Cleaned Items

3. Technical Requirements

3.1 Functional

R1 ..... Frame Transfer mode
R2 ..... Image region 385 x 288 pixels
R3 ..... Storage region 385 x 290 pixels
R4 ..... Non-anti-bloomed

3.2 Mechanical

R5 ..... Package: 20 pin 15.24mm pitch DIL
R6 ..... Fibre stub attached to CCD surface strength 100G @ 4.5g
R7 ..... The thickness of the package including fibre stub shall not exceed 4.2mm
R8 ..... Position accuracies of bonded stub
Parallelism: <3um edge to edge of CCD
Azimuth: +-1 degree
Overlap: min 1mm of stub outside CCD image region

3.3 Electrical

R9 ..... Horizontal pixel shift frequency 10 MHz
R10 ... Vertical frame shift frequency 2 MHz

3.4 Thermal

R11 ... Nominal Temperature 50 °C at which optical requirements shall be met unless otherwise stated.
R12 ... Storage Temperature -50 to +85 °C
R13 ... Operating Temperature 0 to +65 °C

3.5 Optical

R14 ... 22 +- 2um Square pixels
R15 ... Defects
Defect defined as +-2% of average pixel value with filter block
Integration time of 12ms @ Nominal Temperature
Column: none
White spots: none with size >2 pixels
Black Spots: <5
Horizontal: none
R16 ... Defect measurement conditions
Illumination equivalent to half saturation
R17 ... CTE > 99.998%
R18 ... QE > 30% @ 520nm
R19 ... Full well capacity shall be >300 000 electrons.
R20 ... Average dark signal <50 000 electrons per pixel per 120ms @ 50 °C
R21 ... Standard deviation of dark current over all pixels <5% of average dark signal
R22 ... Conversion factor >0.8µV/electron
R23 ... There shall be no hot pixels, defined as >50 000 electrons above the average dark signal with an integration time of 120ms @50°C
R24 ... There shall be <5 warm pixels, defined as >10 000 electrons above the average dark signal with an integration time of 120ms @50°C
R25 ... There shall be no black pixels, defined as <0.95 times average signal.
R26 ... There shall be no hot columns, defined as >1000 electrons/pixel above average dark signal.
R27 ... There shall be no black columns, defined as <0.98 times average signal.

4. Product Assurance Requirements

4.1 Manufacturing and Test Flow

MANUFACTURING AND TEST FLOW
Wafer raw material and epitaxy production
Sample wafer resistivity measurements each epitaxy wafer lot
Device wafer manufacturing and test
Wafer sawing and lapping
Wafer resistivity data each wafer epitaxy lot
Visual inspection, all chips
SEM inspection, each wafer manufacturing lot
Assembly lots
Chip sawing final dimensions
Device assembly
Final Production Tests
Burn-in and screening
Attach fibre block
Assembly lot acceptance
Packaging and Transport

R28 ... Wafer epitaxial layer spreading resistance shall be within 2k Ω.cm and 8kΩ.cm at 25um from the surface measured in accordance with [1].
R29 ... The thickness of the epitaxial layer shall be 50 +- 5um
R30 ... Prior to wafer manufacturing one wafer per epitaxy lot shall be measured for the spreading resistance and layer thickness of the epitaxial layer. All data shall be recorded. Wafers that do not meet the requirements above shall be rejected.
R31 ... After full wafer manufacturing and wafer sawing, a scanning electron microscope inspection shall be carried out on samples from each wafer lot in accordance with the inspection procedure [4] and keeping reference photographs available for later review.
R32 ... A sample of 3 test structure devices from each wafer manufacturing lot shall be tested with a Co60 source for radiation damage.
R33 ... Prior to the assembly of the chip to the support wafer chips shall be inspected for visual defects according to [2] and rejects removed from the lot.
R34 ... One sample each of 3 wafers from each epitaxy lot shall be measured for spreading resistances of the epitaxial layer. If the 3 samples do not give consistent results within 10%, further samples shall be taken such that wafers not meeting the spreading resistance requirements are rejected from the flight lot.
R35 ... From each assembly lot, 3 sample devices shall be tested for destructive wire bond pull in accordance with [10] prior to any further production wire bonding.

4.2 Production Testing

PRODUCTION TESTS

Production and production controls

Production including encapsulation stage

Dimension and alignment check

100% non-destructive bond test on active device bondings

High temperature stabilisation bake

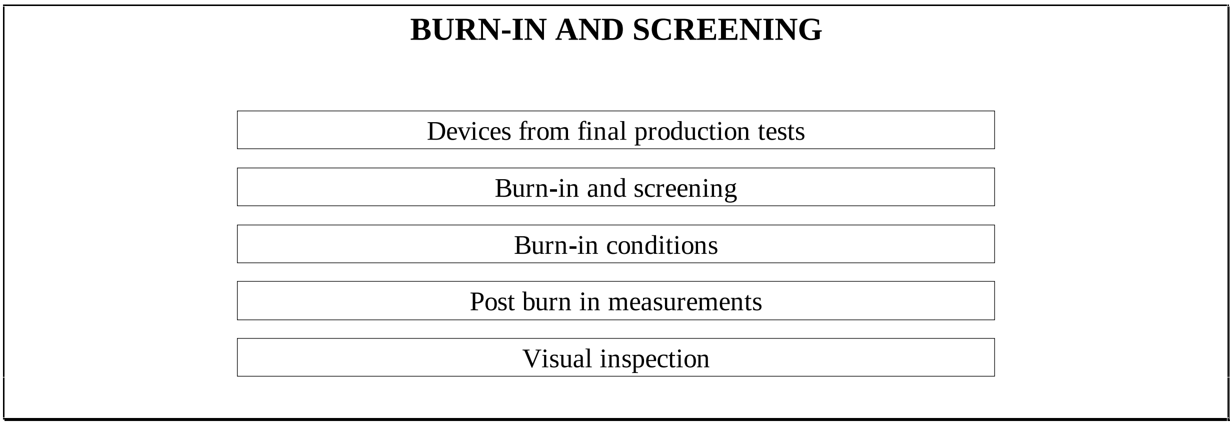
Thermal cycling

Electrical and electro-optical tests

Visual inspection

R36 ... Testing and conditioning shall be carried out in an inert atmosphere (dry nitrogen or vacuum).
R37 ... The mechanical dimensions of packaged devices shall be measured and rejects removed from the lot.
R38 ... The position and alignment of the CCD with respect to the package shall be measured and recorded.
R39 ... All wire bonds shall be tested non-destructively in accordance with [11].
R40 ... High temperature stabilisation bake shall be performed in accordance with [5] during 48 hours at 125 °C.
R41 ... Thermal cycling shall be applied in accordance with [6].
R42 ... Vibration testing shall be performed on 3 samples, after all assembly and conditioning, from each assembly lot in accordance with [9] but at 30G. The lot is passed only if there is no evidence of mechanical damage.
R43 ... Pre burn-in testing shall be defined and performed in order to select devices to meet the post-burn in tests and screening.
R44 ... Devices shall be visually inspected in accordance with [2] and [3].

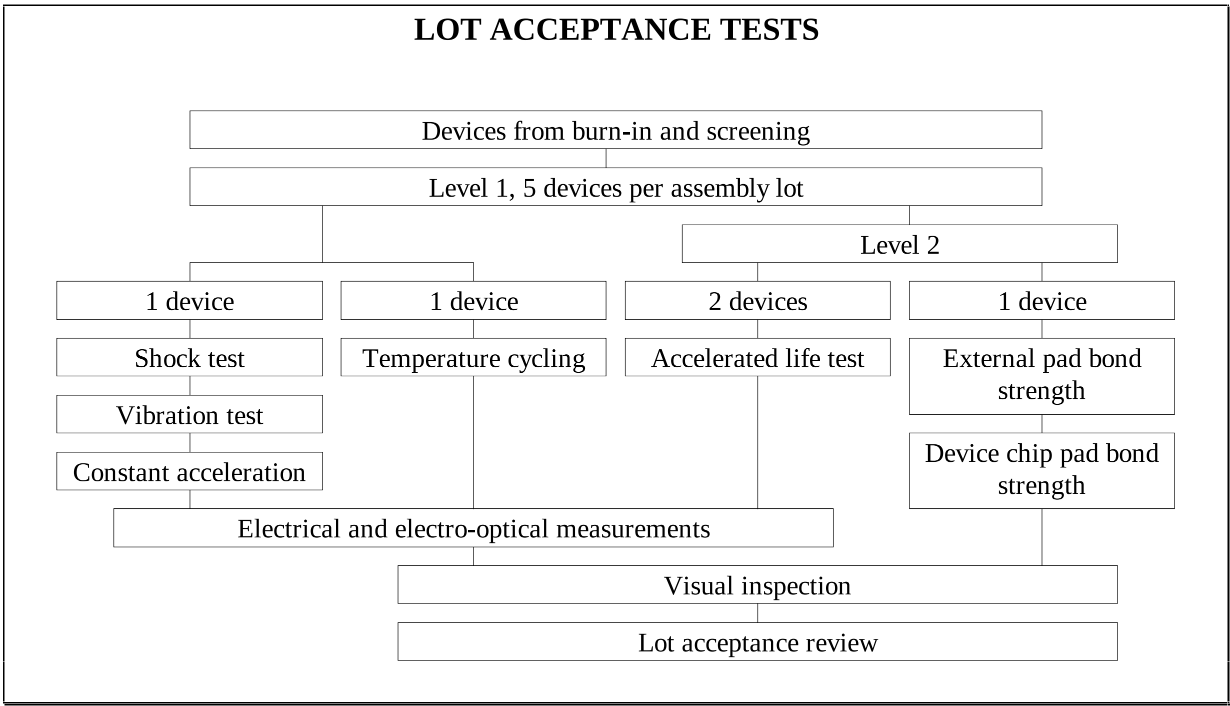
4.3 Burn-In and Screening



R45 ... Burn-In and Screening shall be carried out on devices that have successfully passed the final production tests.
R46 ... All delivered devices shall undergo burn-in and screening.
R47 ... All conditioning, testing and storage of devices shall be in an inert atmosphere (dry nitrogen or vacuum)
R48 ... Burn-in conditions shall be:
Ambient temperature: 125°C
Duration: 168hrs
R49 ... Electrical and Optical test measurements shall be performed after burn-in (post bu rn-in tests) according to the details given in Section 5 “Test Methods and Procedures”.
R50 ... Post burn-in tests shall be performed within 240 hrs.
R51 ... Devices shall be subject to a final visual inspection after the fibre block has been attached in accordance with [2] and [3].

4.4 Lot Acceptance Testing

R52 ... Lot acceptance testing shall be carried out on devices that have successfully passed the burn-in and screening and had the fibre block attached.
R53 ... The sequence and sample sizes for lot acceptance testing shall be as specified in the chart below:



R54 ... All samples shall have gone through burn-in and screening.

R55 ... The shock tests shall be performed according to [8].
R56 ... The vibration tests shall be performed according to [9].
R57 ... The constant acceleration tests shall be performed according to [7].
R58 ... Shock, vibration and constant acceleration tested devices shall undergo a basic functional and performance check that assures that the devices still meet the post burn-in test limits.
R59 ... Accelerated life test conditions shall be:
Ambient temperature: 125°C
Duration: 1000hrs
R60 ... Accelerated life tested devices shall undergo the post burn-in tests and pass the performance criteria.
R61 ... The destructive wire bond pull tests shall be performed according to [10] with post burn-in levels.
R62 ... All bonds in the device shall be tested.

4.5 Marking

R63 ... Each device shall be clearly marked with an identifier that is uniquely referenced to the device's data pack.

4.6 Packaging and Transportation

R64 ... The external packing shall consist of:
An aluminium container with shock absorbing material that may contain several packaged devices.
R65 ... Devices shall be packed individually such as to avoid any damage and deterioration from the transport and storage environment.
R66 ... Individual device packing shall consist of:
An outer heat sealed nylon bag meeting the requirements in [12] Class 3.
An inner heat sealed polythene bag meeting the requirements in [12] Class 1, containing sufficient humidity absorber for 3 months transport and storage.

5. Test Methods and Procedures

5.1 Electrical and Optical Test Methods

1. Integrate 100 frames digitally, full area mode
2. As 1. But vertical clocks stopped, horizontal clock stopped while integrating
3. As 1. But each line is summed after readout to give 1d result, 1 value per column
4. As 1. But clock an additional row and column
5. Derive photon transfer curve

5.2 Optical Test Measurements and Limits

Test No	Parameter	Symbol	Test Method	Notes	Conditions	Limits Min	Limits Max	Units
1	Average dark signal	S_D	1		1		5000	e^-
2	Hot pixels in image and store	N_{HP}	1		1		0	
3	Warm pixels in image	N_{WI}	1		1		5	
4	Warm pixels in store	N_{WS}	1		1		5	
5	Hot pixels in output register	N_{HO}	2		1		0	
6	Black pixels in image	N_{BI}	1		2		0	
7	Black pixels in output register	N_{BO}	2		2		0	
8	Hot columns	N_{HC}	3		1		0	
9	Black columns	N_{BC}	3		2		0	
10	Charge transfer efficiency, image and store	CTE_V	4		4		99.998	%
11	Charge transfer efficiency, output register	CTE_H	4		4[1]		99.998	%
12	Charge to voltage conversion factor	CVF	5		5		0.8	$\mu V/e^-$
13	Output reset noise	S_N	1		1		120	e^- RMS
14	Reset feed through voltage	V_{RESET}	1		1		80	mV
15	Dummy output time constant[2]	τ_D	1	1	1		See Note	ns
16	Signal output time constant	τ_O	1		1		20	ns

Notes:

1. ±10% of signal output time constant.

Conditions:

1. 1MHz, 120ms, 50°C, Dark
2. 1MHz, 120ms, 50°C, Illumination to give 100 000 electrons average signal
3. 1MHz, 120ms, 10°C, Dark
4. 1MHz, 120ms, 10°C, Illumination to give 100 000 electrons average signal on end pixels only
5. 1MHz, 120ms, 10°C, Illumination various levels 100 to 200 000 electrons

[1] Requires no pixel mask on end of row.
[2] If present on the device.

5.3 Electrical Test Measurements and Limits

Test No	Parameter	Symbol	Test Method	Notes	Conditions	Limits Min	Limits Max	Units
1	Leakage current on input gates	I_C	SCC 25000 § 5.1		15V		5	pA
2	Substrate through resistance	R_{SS}	DC Test	1	10mA		100	Ω
3	Forward diode voltages	V_F	DC Test		1mA	0.2	1.5	V
4	Reverse diode leakage currents	I_R	DC Test		24V	50		µA
5	Transistor drain to gate leakage currents	I_{DR}	DC Test		24V	50		µA
6	Gate to gate leakage currents	I_{GG}	DC Test		20V	30		µA
7	Gate protection voltages	V_{GP}	DC Test		30µA	19	27	V
8	Gate input capacitance	$C_{\varnothing}$	DC Test		10V		2500	pF
9	Gate to gate capacitance	$C_{\varnothing M}$	DC Test		10V		1000	pF
10	Output register capacitance	C_O	DC Test		10V		150	pF
11	Reset input capacitance	C_R	DC Test		10V		10	pF

Note 1 : Measured at wafer level only.

5.4 LAT Performance Test

5.5 LAT End of Life Test

6. Programme Requirements

6.1 Deliverables

R67 ... Five parts from an assembly lot that has passed all testing and screening requirements shall be delivered.

6.2 Schedule

R68 ... Parts shall be delivered within 6 months of the placement of an order.

6.3 Documentation

R69 ... Documentation as defined here shall be made available at the delivery review prior to delivery and shipment.

R70 ... All documentation packages shall be identified with
Reference to device specification and issue
Reference to purchase order and date
Device serial numbers, assembly lot, and wafer manufacturing lot.

R71 ... A data pack shall be provided for each device including
Device wafer traceability
Production test measurements
Post burn-in test measurements

R72 ... A data pack shall be provided for each wafer manufacturing lot including
Wafer production report

R73 ... A data pack shall be provided for each assembly lot including
Device and wafer traceability
Failure analysis reports
Lot acceptance test report