Document Title: **Instrument Controller Design Description.**

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Contents

1. Change History

Draft 1	First Version For Internal Comments. 3 February 95.
Issue 1	16 February 95. Description of M3DS2 Board.
Issue 2	4 October 95. Description of EM IC PCB.
Issue 2.1	25 October 95. Description of EM IC PCB. Clock baseline @8MHz.
Issue 3	17 July 96 EQM
Issue 4	8 January 97 Various small updates, fill section 8 and 9
Issue 5	12 May 99 Comment on SW delay for reading time in section 7.3 IC Procedure For Reading Time From The RBI

2. Applicable Documents.

RGS-MSSL-IC-001	Instrument Controller Design Specification
Drawing MSSL A1/5230/005 Issue 2	XMM RGS Instrument Controller
RGS-MSSL-IC-004	Instrument Controller Subsystem Interface Timing Specification
RGS-MSSL-IC-005	Instrument Controller PCB Test Procedure
ESA-SCC/9544006	OBDH-Remote Bus Interface RBI Circuit, Based on type HAF_12663

GPS SOS Radiation Hard Hi-Rel IC and ASIC Handbook July 1995 containing:-

MA31750 Data sheet.	
MA31750-Apps Note 11	Bus Arbiter.
MA31750 Apps Note 14	Use of NMA31750 Samples.
54HSC/T Series	High speed CMOS/SOS Logic.

3. Glossary and Conventions.

APID	Application Identifier
CCD	Charged Coupled Device

CDMU	Central Data Management Unit
CMD	Command
CSG	Clock Sequence Generator
DBI	Digital Bus Interface
DBU	Digital Bus Unit
DMA	Direct Memory Access
DPP	Data PreProcessor
EMC	ElectroMagnetic Compatibility
EOS	End Of Sequence
GPS	GEC Plessey Semiconductors
HC	Heater Control
HK	House Keeping
IC	Instrument Controller (RGS)
ICU	Instrument Control Unit (OM)
I/O	Input/Output
MMU	Memory Management Unit
MSSL	Mullard Space Science Lab
M3DS	MSSL 31750 Development System
M3DS2	MSSL 31750 Development System Version 2
M3RGSIF2	MSSL 31750 RGS InterFaces for version 2
OBDH	On Board Data Handling
OM	Optical Monitor
PCU	Power Conditioning Unit
PROM	Programmable Read Only Memory
RAE	RGS Analogue Electronics
RAM	Random Access Memory
RBI	Remote Bus Interface
RDE	RGS Digital Electronics
RFC	RGS Focal Camera
RGS	Reflection Grating Spectrometer
ROM	Read Only Memory
RTU	Remote Terminal Unit
SCET	Spacecraft Elapsed Time
SOS	Silicon On Sapphire
S/C	SpaceCraft
TBD	To Be Determined
TC	Telecommand
TM	Telemetry

4. Introduction.

This document describes the hardware design of the RGS RDE IC.
The design is housed on a RDE format board, defined in MSSL drawing A2/SK/1097.
The design has drawn on the experience of developing the M3DS, M3DS2 and EM boards.

The IC interfaces to the S/C's OBDH bus via the RBI, DBI and DBU. The RBI is housed on the IC PCB and the DBU is an external unit powered from the RDE. The RBI uses DMA cycles into the IC's RAM to communicate with the IC. The IC's software takes care of the protocol used for this interface, both for telecommands and telemetry.
The IC interfaces to three subsystems internal to the RDE, the DPP, PCU and HC via a back plane in the RDE box. Although functionally a part of the IC, the digital interfaces to the RAE are accommodated on the DPP "Front End" card. These interfaces are the Command and Housekeeping interfaces, the End Of Sequence signal (EO_SEQ), a single signal and the Pixel Data interface. The PCU contains a DC/DC convertor which conditions the S/C's raw power bus. The PCU then switches and monitors the secondary power rails under control of the IC. The HC is housed as part of the PCU which is used to control the CCD cold bench temperature in the RFC.

The IC uses a MA31750 processor.

The RBI is a MC1031 Standard RBI chip as used on Envisat, ESA SCC/9544006.

All 54HC series logic parts used in the design are available in the GPS SOS Radiation Hard Hi-Rel Integrated Circuit and ASIC Handbook, July 1995.

The RAM to be used for flight is Honeywell's HC6856 32K*8 Radiation-Hardened Static RAM.

The PROM to be used for flight is Raytheon Semiconductor's R29791 8K*8 bipolar PROM.

The software for the IC is written in assembly language for the Bootstrap and in ADA for the Application code.

The processor clock speed is 8MHz. No wait states are added for memory accesses, one is added for IO accesses. The RBI uses a 4MHz clock.

5. Design Description

The circuit diagrams for the IC are found in MSSL drawing number A2/5230/005.
The design can be split into three basic blocks, the Spacecraft interface and bus arbiter, the memory and the processor.
Below is a description of the content of these three blocks.
The IC is designed to run with a backplane supply voltage of 5.1(+/-0.1)V. The IC uses this supply directly from the backplane with two exceptions.

One, the ROM's, the power to these are switched due to the high power consumption of the devices. The software must turn off these devices within two seconds of initialisation. The flight PROM's typically demand 160mA each.

Two, the RAM's, the power to these is "OR'ed" with the Keep Alive Line (KAL). The KAL is regulated in the PCU subsystem.

5.1 Spacecraft Interface and Bus Arbiter (SIBA).

(MSSL A1/5230/005 Sheet 1 of 3)

The Spacecraft interface is based on the Envisat RBI, MC1031. For a full description of this device refer to ADV's data sheet, MC1031 Standard RBI Chip For OBDH Interface and ESA's SCC Detail Specification No. 9544/006, Integrated Circuit, Monolithic, CMOS Silicon On Sapphire, OBDH-Remote Bus Interface Circuit, With 3-State Outputs, Based On Type HAF_12663.

The DBI, spacecraft interface, enters the RDE via a 37 way female D-Type connector. The digital signals are filtered using RC networks and buffered, using 54HC14's and 54HC244's.

The USERAD, the User address on the OBDH bus, is link selectable by links on the external harness mating connector, using the RDE supplied signals DIGREF1 and DIGREF0 to determine the address on RBIAD0-4. The APID, the Application Identifier used by software, is also link selectable by the same means, see APID0-1 on the D-Type. This allows the four flight RDE units to be identical.
The RGS1 USERAD is 10010 bin and for RGS2 is 10100 bin.
The RGS1 APID is 01 bin and for RGS2 is 10 bin.

The RBI clock speed is set to 4MHz for a system clock of 8MHz. The RBI clock speed has a maximum specified frequency of 5MHz.

The RBI uses DMA cycles to transfer information to and from the IC. To achieve this, logic is

included to perform the bus arbitration function. For a full description of its function see GPS's application note 11.
The RBI's arbiter can not be used with this processor due to features of the MA31750.
Half of a 54HC244 is used to source signals not produced by the RBI during DMA cycles which the system requires, these are DSN, RDWN, MION and OIN. A link is supplied on the input to the 244 from the RBI to enable IO space to be accessed via the RBI for ground testing purposes. This link will be out under normal circumstances so only the memory is accessible to the spacecraft.

Six interrupt sources from the RBI are utilised.
RESETMCN is combined with other signals in the Processor block to generate a power down non maskable interrupt. 256uS later a system reset will also be generated. This is described in more detail in the Processor section.
BCP4 is a dedicated interrupt source used during the time verification procedure under control of the spacecraft.
IT1N, instruction to RBI, IT2N, instruction to User, and IT_LOSSN, OBDH clock loss, are combined together as as one interrupt to the processor. The processor can determine the source of the interrupt by reading the RBI's configuration register. Bits 8 and 9 are set if IT1N or IT2N have been asserted and if neither are set then IT_LOSSN has been asserted. (IT_LOSSN can occur with in 305uS of an IT interrupt.)
The RBI's watchdog function is used, IT_WAT is connected to the processors power down interrupt and reset circuit in the Processor Block. This signal is functionally ORed with the RESETMCN signal.

The RBI's two time Freeze registers are implemented.
Freeze register one is used by the instrument to freeze the time at which a clock sequence read out finished. The EO_SEQ signal from the CSG, via the DPP, is joined to EXT_FR1.
Freeze register two is used by only by the IC's software to sample time. The time is latched by the processor writing to the RBI's configuration register. Freeze register two is used in time synchronisation and verification procedures.

The generation of wait states for the RDE system is performed in this block. The signal used by the processor to sense wait states is called RDYN.
There are three sources of RDYN: accesses to memory, I/O space and the RBI.
A signal MEMRDYN produces RDYN for the memory. A signal SUREN, start up ROM enable, is used to make this longer for the ROM when the ROM is enabled. This also allows for testing with a ROM emulator. When accessing RAM no wait states are added.
A signal IORDYN gives RDYN for all the processor's accesses to I/O space, except the RBI which generates its own RDYN, RBIRDYN. I/O space other than the RBI uses one wait state.

A 54HC138 in this block decodes I/O space for the system. The processor's Address Strobe line is included in the decoding which excludes glitches on the decoded lines. There are three areas of I/O space described below.
The signal APIDN enables the software to read the APID for the unit, the signal also gates IORDYN to RDYN using a 54HC125 gate. The APID is read on the least significant two bits of the data bus.
A signal RBICSN enables accesses to the RBI and enables the RBI's own RDYN. The RBI has an address space of 16 locations. The operation of these 16 registers is defined in the MC1031 data sheet.
The signal IODECN is used to address the RDE's subsystems and is used to enable IORDYN. IODECN is further decoded within the Processor block to address the individual subsystems, namely the PCU, HC and DPP.

5.2 The Memory Block (MEM).
(MSSL A1/5230/005 Sheet 2 of 3)

The memory system contains 128K Words of static RAM which is write protected during power up and power down conditions. The RAM content is also maintained by the Keep Alive line when the S/C power bus to the instrument is off.

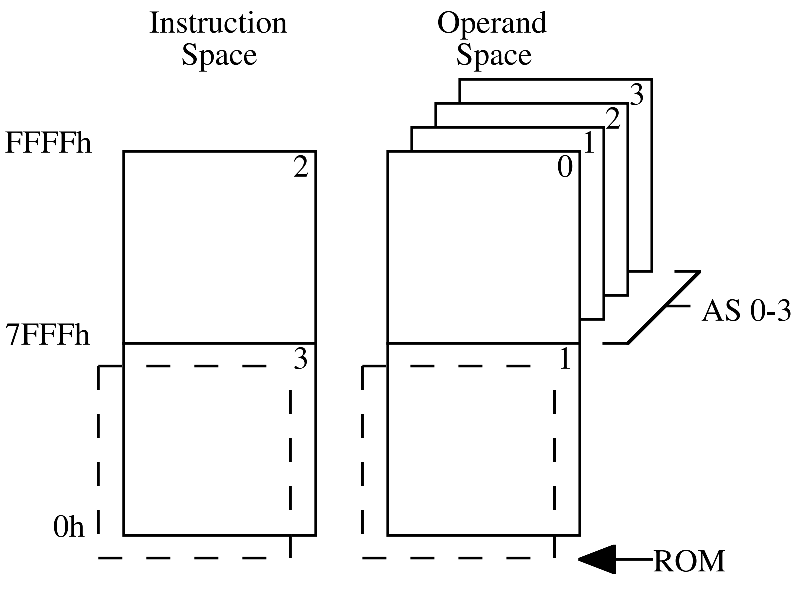
A LM119 in this block is used to monitor the condition of the 5V rail. When the 5V rail is below a certain level a signal PWROK is low. The falling edge of PWROK interrupts the processor on its PWRDN interrupt. The processor is required to use this to run a small routine safing the instrument and saving its state before power down.

WRENABLE is a signal derived from PWROK that inhibits chip selects to the RAM, hence disables writes to the RAM chips. This signal, on power up, inhibits the RAM chip selects until power is OK. On power down, the RAM can be written to until a signal RESETN becomes active. RESETN will be generated some time after PWROK goes low (the generation of RESETN is described in the Processor block).

The 54HC logic in this block is powered by the normal 5V rail.
The RAM's are powered from a circuit containing transistors which "OR" together the system 5V and the Keep Alive Line, both from the backplane. The RAM's chip selects are pulled high to this "OR'ed" supply.

The processor has an address space of 64K words. To give enough area for the application code and working space for data, the processors OIN (operand instruction) control line is used to switch between two 64K words pages. Each page can be seen as two 32K word Areas, two in instruction space and two in operand space.
Areas “3” and “2” are in instruction space and are read only.
Areas “1” and “0” are in operand space and are read/write accessible.
In addition Area “0” can be switched to any one of the four 32K Word Areas by manipulating the Address State of the MA31750 processor. An Address State of three would put Area “3” in the top half of the operand space, etc. The Address State is normally “0”.
On power up the bottom half of both operand and instruction space, when performing read cycles, are overlapped by the start up ROM’s. Whilst the ROMs are enabled, using the address state of the processor, the whole of the RAM can be accessed during both read and write cycles in the top half of operand space, Block “0”. This allows the application code to be set up in the RAM before the ROM is switched off.
This decoding scheme is shown diagrammatically below.

Figure 1. **Memory Map**



5.3 Processor (PROC).
(MSSL A1/5230/005 Sheet 3 of 3)

This block includes the MA31750 processor, decoding to read the Start Up ROM’s, the Reset circuit, the Configuration register, the system oscillator, and clock dividers.

The Reset circuit is designed to produce a system reset on power up and to give a reset 256uS after a PWRDN interrupt. Activation of PWROK, a signal from the Memory block, RESETMCN, from the RBI or an IT_WAT, from the RBI's WatchDog timer, will produce a PWRDN interrupt. The logic for RESET delays RESETN to the system so the processor can complete its write operations and run a small routine saving the software state.

On power up the processor reads the Configuration register (CONFWD on the schematic) to determine the system configuration. The schematic shows how the bits of this register are set up.

The oscillator used is a single transistor Pierce type. It can be used in the range 5-20MHz with one set of component values.

Two 54HC163 devices divide down the oscillator to give a choice of frequencies. The values shown on the schematic are for a 16MHz crystal.

ROMs are used to store the bootstrap and Check Out Code.
The circuit is designed for 16K Words of ROM.
On power up of the system, the ROM's will turned on with the system reset signal. The ROM's are turned off when SUREN goes inactive under software control. RESETN is used to turn on the ROM's to give them long enough to turn on because the time from SUREN active to the first access cycle is not long enough. If the ROM's are turned on again under software control the software must delay accesses to the ROM. Four transistor circuits individually supply power to each ROM chip.
Buffering of control and bus lines is provided to isolate the ROMs from the system busses when turned off.
An 8 pin header provides the flexibility to use the ROM emulator and different types of ROM during development work.
The ROM's use sockets on the board layout.
On power up SUREN will be active and the processor will "see" the ROMs in the bottom half of its 64K memory. When SUREN is disabled the processor will run code from its RAM.
When the ROM's are enabled a 54HC138 supplies decoding to supply a signal ROMRDN to enable the data buffers to the ROM chips. This signal is valid when the processor is performing a read cycle from the lower half of memory (MION is high, A0 is low) with SUREN active.
SUREN is a discrete signal from the processor meaning: Start Up ROM Enable Not.

This block includes the connector used for the backplane, a Hypertac 120 way male right angle pin connector SCC 3401/016.

To interface to the backplane buffers are used for the data, address and control lines.
A 54HC138 decodes space for the individual RDE subsystems.
A second 54HC138 supplies a modified write strobe for the interfaces. This is designed to give an improved data hold time after the end of the strobe. Detailed timing is given in RGS-MSSL-IC-004, Instrument Controller Subsystem Interface Timing Specification.

Links are included for the interrupt lines to the processor. This allows for future changes and enables the interrupts to be physically disabled during the commissioning phase of the board.

PWRDN	This is the power down interrupt.
INT02n	Linked to CMD_GT, the envelope signal for the RAE Command interface. This gives the option of the falling edge of the signal causing an interrupt indicating the end of a command transfer. This source may not be used if the software just polls this interface.
INT08n	Linked to BCP4. This signal is sourced by the RBI chip. BCP4 is used in the time verification procedure, indicating to the processor when time is to be latched into the RBI's EXT_FR2 register. The IC shall read this value and telemeter it to the ground in a time verification packet.
INT10n	Linked to EO_SEQ. This signal is sourced in the RAE from the CSG, indicating the end of a CCD read out sequence. This signal is also link selectable to latch the time in the RBI's EXT_FR1 register. This will give an accurate time for the end of a read out.
INT11n	Linked to HK_REQ, the envelope signal for the RAE Housekeeping interface. This gives the option of the falling edge of the signal causing an interrupt indicating the end of a housekeeping transfer. This source may not be used if the software just polls this interface.
INT13n	Linked to RBIINTN. This signal is derived from IT1N, instruction to RBI, IT2N, instruction to User, and IT_LOSSN, OBDH clock loss. This interrupt is used in communications with the spacecraft.
INT15n	This interrupt is spare.

All links are fitted except INT02n and INT11n.

The processor's other interrupts are not used.

6. I/O Address Map.

Name	Base Read	Base Write	Number Of Locations
APIDN	E000h	Read Only	1
RBICSN	E800h	6800h	16
PCUN	F000h	7000h	16
DPPEN1N	F100h	7100h	16
DPPEN2N	F200h	7200h	16

7. Software Operations.

7.1 APIDN, the Application Identifier.

The APIDN area is used to read the APID, the Application Identifier, used by software to determine which RGS instrument it is, RGS-1 or RGS-2. The software will read from this location, using the least significant two bits D14 and D15 to determine the APID. D14 is APID 0 and D15 is APID 1, the least significant bit.

7.2 Time Synchronisation And Verification Procedures.

Time Synchronisation.

7.2.1) TC(10,1) will be sent from the ground to the spacecraft telling the CDMU to synchronise time for an instrument.

7.2.2) The CDMU will send TC(10,2) to an instrument informing it that its local time is to be synchronised to the SCET. The TC's APID determines which instrument is to be synchronised.

7.2.3) The instrument enables time synchronisation to occur by commanding the RBI. To do this is writes 1000hex to the RBI configuration register, address 6806 hex. Also the instrument sets a "flag" (available via HK-TM) to indicate that it is undergoing time synchronisation. The RBI time is still valid or at least useful. The command to the RBI can be verified by reading the Configuration register E806 hex and checking that bit 11 is set, indicating timer reset is enabled. This bit is reset when the time synchronisation sequence has occurred.

If a time tagging operation takes place during the synchronisation process or even immediately after the RBI counter reset, the actual counter value shall be used to generate a Time Field, instead of generating a dummy time via software (It is MOC/SOC responsibility to take care of possible time corrections needed).

7.2.4) At least 100mS later the CDMU generates a BCP3, BCP2 sequence. This resets the RBI time to zero. At the same time the CDMU takes a copy of the SCET. The RBI continues to count from zero.

7.2.5) Within a second the CDMU generates TC(10,3) "Add time code packet". This contains the copy of the SCET taken in 4). The packet time format used is the XMM standard 6 octet format with 4 octets of coarse time and 2 octets of subseconds

7.2.6) The instrument takes the 48bit copy of SCET and discards the least significant 8 bits. The next 32bits are written into the RBI, the most significant 16bits into the RBI register 0C hex and the least significant 16bits into register 0D hex. On the second write the RBI chip adds the value to the time value it has reached since the BCP3, BCP2 sequence.The remaining 8 bits of the SCET are kept in the instruments memory.

Note that the user shall take care that no freeze operation on the Freeze 2 register occurs between the loading of register 0C hex and register 0D hex.

7.2.7) The instruments time is now valid. The "flag" set to indicate that the local time is not valid can now be reset.

Time Verification.

7.2.8) The ground generates TC(10,4), sending it to the CDMU.

7.2.9) The CDMU will send TC(10,5) to an instrument informing it that its local time is to be verified. The TC's APID determines which instrument is to be verified.

7.2.10)The instrument sets a "flag" (available via HK-TM) to indicate that it is undergoing time verification.

7.2.11)The CDMU generates a BCP4 pulse after a delay of at least 100mS, at the same time taking a copy of SCET. In the instrument the BCP4 pulse generates an interrupt.

7.2.12)The CDMU generates a TM(10,4) packet, containing the copy of the SCET at the time of the BCP4 pulse.

7.2.13)The instrument, on reception of the BCP4 interrupt, acquires time from the RBI Freeze register 2 having written 80hex to the RBI's configuration register.

Using this value and the value held in memory, the instrument builds the time field for a TM(10,5). Local time is sent in TM(10,5), the Time verification report packet.

7.2.14)The instrument, having dealt with the BCP4 interrupt, can reset the time verification flag. Normal time operation can resume.

Note that during the time verification procedure that the BCP4 interrupt routine may interfere with normal time tagging operations. This will come about if the BCP4 interrupt occurs after the normal time tagging operation has latched time but has not yet read it. It could be said that the error in the normal time tagging operation will be small. The actual time in TM(10,5) will have an error due the software latency of the interrupt routine. This error could be said to be small since the verification process will occur when limited software functionality is enabled.

7.3 IC Procedure For Reading Time From The RBI

When “freezing” time with the RBI chip, a one OBDH clock period delay should be observed between the freeze operation and reading the freeze registers. This will guarantee a valid time. This delay should be observed for both software freeze time commands and hardware External freeze commands.
The OBDH clock period is 1.9uS (524288 Hz).

Procedure For Reading Time.

Send Freeze OBT (On Board Time) command 80 hex to the RBI chip configuration register. This latches the timer counter value in the external freeze 2 register.

  Write 80 hex to IC I/O address 6806 hex.

The XMM Packet Time Format uses six octets. The instrument creates this format as follows:

  The most significant octet is held in memory.

  The next two octets are read from the RBI External Freeze 2 register (bit 0-15).

    Read 16bits from IC I/O address E80C hex

  Then two octets are read from the RBI External Freeze 2 register (bit 16-31).

    Read 16bits from IC I/O address E80D hex

  The least significant Time octet is read from the RBI External Freeze 2 register (bit 32-42) using the most significant octet.

    Read ms 8bits from IC I/O address E80E hex

Procedure For Time Stamping CCD Frames

For time stamping CCD frames with 1.9uS accuracy a similar procedure to the above is followed except RBI External Freeze 1 is used and in the last case where eleven bits are read rather than eight.

The EOS signal latches the time in the RBI and causes an interrupt to the processor INT10. The IC software in answer to the interrupt does the following.

The most significant octet is held in memory.

The next two octets are read from the RBI External Freeze 1 (bit 0-15).

Read 16bits from IC IO address E809 hex

Then two octets are read from the RBI External Freeze 1 (bit 16-31).

Read 16bits from IC IO address E80A hex

The least significant eleven bits of Time are read from the RBI External Freeze 1 (bit 32- 42) using the most significant eleven bits.

Read ms 11bits from IC IO address E80B hex

Note the IC software should follow this procedure before the next interrupt arrives otherwise the latched time will be over written by the new interrupt.

7.4 Non Conformance And Corrective Action of RBI Chip in On Board Time.

The RBI chip has a known none conformance in its time operations.

If one thinks of bits 32-42 of the time value as an eleven bit counter, the transition from 3ff hex to 400 hex increments bits 0-31 rather than the transition of bits 32-42 from 7ff hex to 000 hex. (ie Bit 31 of the time is incremented on the setting of bit 32 rather than the reseting of this bit.)

The counter acts as follows (starting from power up):

0, 1, ..., 3FE, 3FF, C00, C01, ..., FFF, 800, 801, ..., BFF, 1400, ..., 17FF, 1000, ...

instead of

0, 1, ..., 3FE, 3FF, 400, 401, ..., 7FF, 800, 801, ..., BFF, C00, ..., FFF, 1000, ...

The corrective action to be implemented in software is as follows:

IF bits 32-42 > 3FF hex THEN bits 0-31 = bits 0-31 - 1

or

IF bits 32-42 > 3FF hex THEN time value = time value - 800 hex.

7.5 RBI Interrupt Sources.

IT1N, instruction to RBI, IT2N, instruction to User, and IT_LOSSN, OBDH clock loss, are combined together as as one interrupt to the processor. The processor can determine the source of the interrupt by reading the RBI's configuration register E806 hex. Bits 8 is set if IT1N has been asserted and bit 9 if IT2N has been asserted and if neither are set then IT_LOSSN has been asserted. (IT_LOSSN can occur with in 305uS of an IT interrupt.)
IT2N , instruction to User,

7.6 Watch Dog Operations.

The RGS will use the RBI's Watchdog timer, a twelve bit counter clocked by a 256Hz clock derived from the OBDH clock. This timer can give a programmable time out from 3.9mS to 16 seconds. If the timer reaches zero a PWDN interrupt is generated, 256uS later the IC will be reset. This timer is disabled on power up and is enabled by IC software. If the IC is suspended by the S/C this timer is stopped. When the IC is allowed to continue the watchdog timer will resume from where it was stopped. The timer can be enabled and disabled by IC software commands to the RBI's configuration register. The time out period is programmed by writing to the RBI's Watchdog Register, a value of FFF hex will give the longest time out period. The action of the write loads the value into the timer.
Here are the software IO commands to be used:
Write 100 hex to IO address 6806 hex to enable/disable the watchdog.
Read bit 15 of IO address E806 hex to check watchdog enable state.
Write a value between 1 hex and FFF hex to 6808 hex, the Watchdog Register.

For information only a description of the Processor's Watchdog function is given.
The MA31750 processor used in the IC has an in built counter called the Trigger-Go Counter. This 16 bit counter is clocked by a 62.5KHz clock connected to the TCLK pin of the processor (This clock is derived from the IC's 16MHz crystal). It is enabled during system initialisation and its time out period can be varied using the Trigger_Go Reset Register. On initialisation the counter value is zero. When the counter overflows, is used, a PWDN interrupt is generated and 256uS later the RDE would be Reset.
Using the Trigger_Go Reset Register the time out period can be varied from 32uS to 1.05 seconds, a value of zero gives the maximum time out period. Issuing the Reset Trigger-Go command will reset the time to that held in the Trigger_Go Reset Register. The Trigger_Go Reset Register value is zero on power up.
There is no means to disable this counter.

Here are the software IO commands to be used:

	Mnem	Code	
Reset Trigger-Go	Go	400B hex	
Output Trigger-Go Reset Register	OTGR	040E hex	Write a 16 bit value
Input Trigger-Go Reset Register	ITGR	840E hex	Read a 16 bit value

8. Low Level Accesses Of The IC's Memory By The Spacecraft.

The whole of the IC's memory can be accessed.

The RBI's Page address and Start address registers map the the processors address lines and address state lines as follows, where AS0-3 are the address state lines, A0-15 the address lines and x are "don't care". (Note: the Base Address register will overlay the Page Address register for Immediate Read instructions and Reset Page Address Instructions.)

Page Address

RBI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Proc	x	x	x	AS0	AS1	AS2	AS3	A0	A1	A2	A3	A4	A5	A6	A7	A8

Start Address

RBI	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Proc	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	note1

Note 1: For flight this bit is "don't care", x. For unit testing on the ground this line is used to access IO space, a one here selects memory, a zero selects IO space (A link is fitted for this purpose to MION ("Memory, Input/Output Not")).

As shown above the processor address lines are offset by one. This is because the RBI accesses memory one word at a time and increments it's address by two each time, so RBI bit 15 of the Start Address is not used.

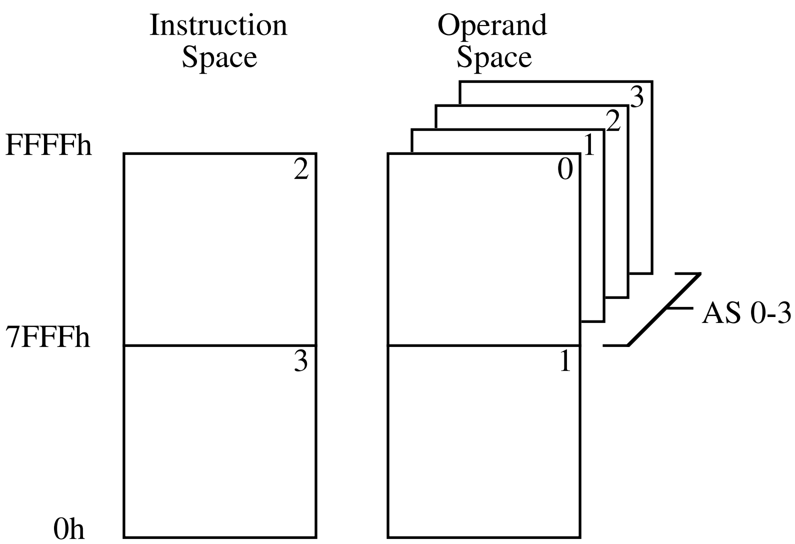
The processor has an address space of 64K words. To give enough area for the application code and working space for data, the processors OIN (operand instruction) control line is used to switch between two 64K words pages. Each page can be seen as two 32K word Areas, two in instruction space and two in operand space, as shown below in figure 2.
The RBI can directly see the whole of the Operand Space, areas 0 and 1, using the RBI register bits that correspond the processors A0 to A15 lines
In addition Area "0" can be switched to any one of the four 32K Word Areas by manipulating

the Address State lines indicated as AS0 to AS3 above.
For example An Address State of three (0011bin for AS0-3) would put Area “3” in the top half of the operand space. At the same time A0 would need to be set to a one and then A1 to A15 can be manipulated to address the 32K word block. Table 1 shows the setup to access all four of the areas.

Table 1

Area Address State	Page Address Register (Hex)	Start Address Register (Hex)	
0	0100	0-FFFE	Top half of operand/data space.
1	0200	0-FFFE	Bottom half of operand/data space.
2	0500	0-FFFE	Top half of instruction space.
3	0700	0-FFFE	Bottom half of instruction space.

Figure 2.



9. High Level Accesses Of The IC’s Memory By The Spacecraft.

The IC’s software will setup the RBI’s Base Address Register for use by the spacecraft to communicate with the IC’s communication area (CCA).
The spacecraft and IC shall never use bits 0-6 of the Base Address or Page Address register for normal TC/TM interactions and these bits shall be zero.